DAS-429PCMCIA/RT10
DAS-429PCMCIA/RT6D4

for

ARINC 429 and Discrete
Test and Simulation Cards

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

Chapter 1 provides an overview of the *DAS-429PCMCIA/RT10* and the *DAS-429PCMCIA/RT6D4* avionics communication cards. When reference is made to both cards, the notation used is *DAS-429PCMCIA/RT[D]*.

This *User's Manual* supports both cards. All references are to both cards, unless otherwise indicated. For a description of the registers unique to the *DAS-429PCMCIA/RT6D4*, see **Chapter 5: DAS-429PCMCIA/RT6D4 Operation & Control Registers**. For the adapter cable connector pinout difference between the RT10 and the RT6D4, see **Chapter 6: Mechanical and Electrical Specifications**.

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1.1 Overview

The *DAS-429PCMCIA/RT10* and the *DAS-429PCMCIA/RT6D4* are ARINC 429 multi-channel, interface cards for PCMCIA systems.

Both cards contain 68 Kbytes of true dual-port RAM, for data blocks, control registers and Look-up table, mapped within the Common Memory space. The card also provides a Card Information Structure (CIS) within the Attribute Memory space.

The cards comply with the Personal Computer Memory Card International Association (PCMCIA Release 2.1) standard, including Plug and Play. The card's small size and suitability for PCMCIA compatible notebook computers with Type II and Type III slots make it a complete solution for developing and testing ARINC-429 interfaces and for performing system simulation of the ARINC-429 bus, both in the lab and in the field.

The cards come complete with GUI software, a C-driver software library including the source code and an adapter cable assembly.

DAS-429PCMCIA/RT10

The *DAS-429PCMCIA/RT10* card supports ten ARINC channels – six programmable as transmit or receive and four receive only. Each of these channels feature error injection and detection capabilities.

The receive channels allow for the storage of all selected Labels with status and Time Tag information appended to each word. The receivers allow for filtering and multi-storage modes of Data Words.

The transmit channels operate via a transmit 'instruction stack' which allows scheduling of data transmissions and reduces the need for host computer intervention.

DAS-429PCMCIA/RT6D4

The *DAS-429PCMCIA/RT6D4* card supports up to six programmable ARINC 429 channels as above for the *DAS-429PCMCIA/RT10*. In addition the card supports any combination of four bidirectional input and output discrete channels. Input channels are user-selectable to TTL (0–5V) or Avionics (0–32V) voltage levels. Output channels are open collector, capable of handling up to 32V with a maximum sink current of 100 milliamperes each.

The discrete channels contain control registers that are memory mapped and can be accessed in realtime.

For ordering information see **Chapter 7: Ordering Information**.

1.1.1 Card Features

General Features

- RT10:
  - 6 ARINC 429 channels configurable as Tx or Rx
  - 4 ARINC 429 Rx-only channels
- RT6D4:
  - 6 ARINC 429 channels configurable as Tx or Rx
  - 4 Discrete I/Os configurable as input or output
- Memory Mapped, 64K x 8 dual-port RAM
- Programmable per channel:
  - Buffer size, Bit rate, Parity
- Programmable hardware output trigger (optional)
- Interrupt and polling modes
- PCMCIA Type II PC card (Plug and Play)
- Ruggedized cable connection

ARINC 429 Transmit Channel

- Three transmit modes:
  - One-shot, N-times, Loop
- Programmable gap time between words/blocks
- Error injection per block:
  - Bit Count Hi/Lo, Sync Time, Stretch Bit, Bit Rate, Parity

ARINC 429 Receive Channel

- Three receive modes:
  - Look-up table
  - Sequential per channel
  - Sequential merge
- Word status tagging
- 32-bit word Time Tagging
- Label/data filtering
- Start triggers
- Receive error count per channel
- Receive count interval trigger
- Error detection per word:
  - Bit Count, Sync Time, Parity, Bit Coding

Discrete Input

- Software selectable voltage threshold:
  TTL 0 – 5V or Avionics 0 – 32V
- Programmable trigger mask
- Interrupt on changing input

Discrete Output

- Open collector outputs (0 – 32 V)
- Drive capability up to 100mA sink current per discrete

Physical Characteristics

- Dimensions: 85.6mm x 54mm x 5mm (PCMCIA type II without cable)
- Weight: 59 g

Operation Environment

- Temperature: 0° to 70°C standard temperature
  -40° to +85°C extended temp. (optional)
- Humidity: 5%–90% noncondensing

Host Interface

- PCMCIA compliance: PCMCIA release 2.1
- Memory space occupied: 64 KB Common Memory
  4 KB Attribute memory
- Power: 5V @ 860mA (6 Tx)

Software Support

- C drivers with source code
- Mystic software for Windows
- *Exalt Plus*: Excalibur Analysis Laboratory Tools (optional)
- Additional software may be available on our website

For exact part numbers see **Chapter 7: Ordering Information**.

1.1.2 Block Diagrams

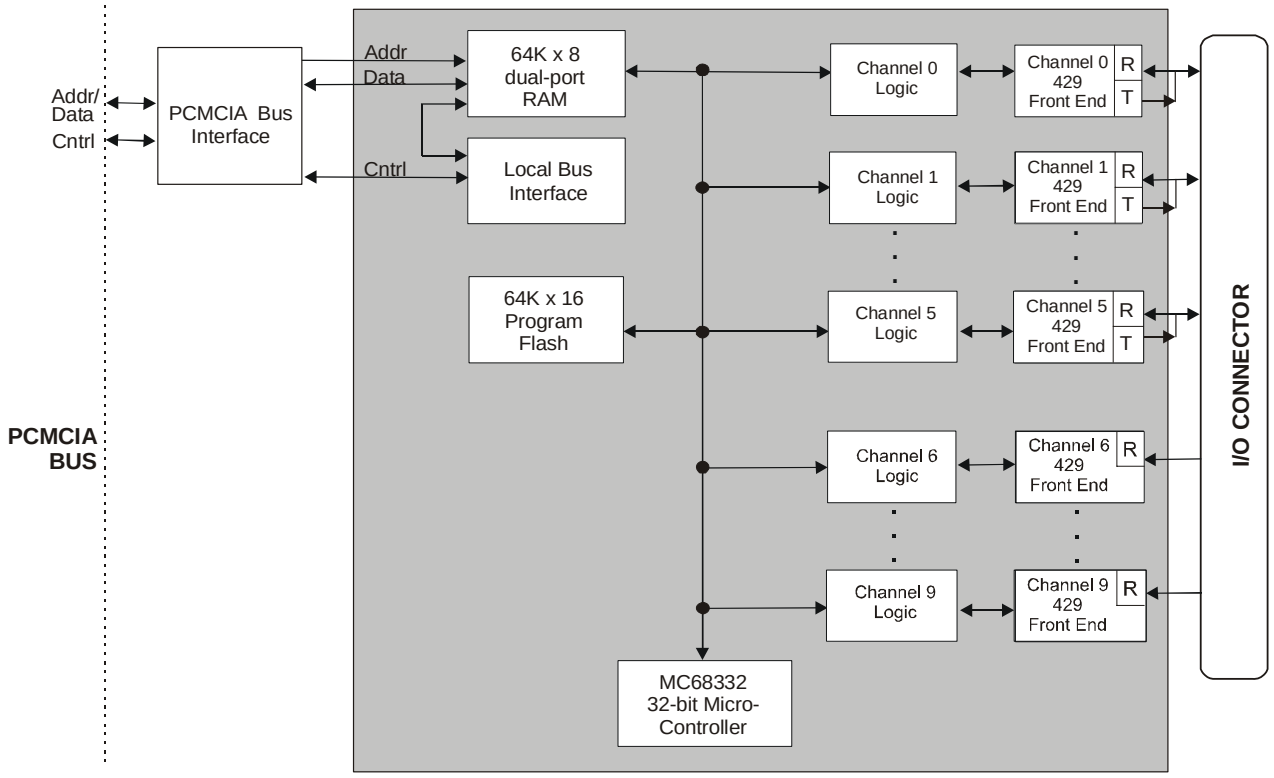

Figure 1-1 DAS-429PCMCIA/RT10 Block Diagram

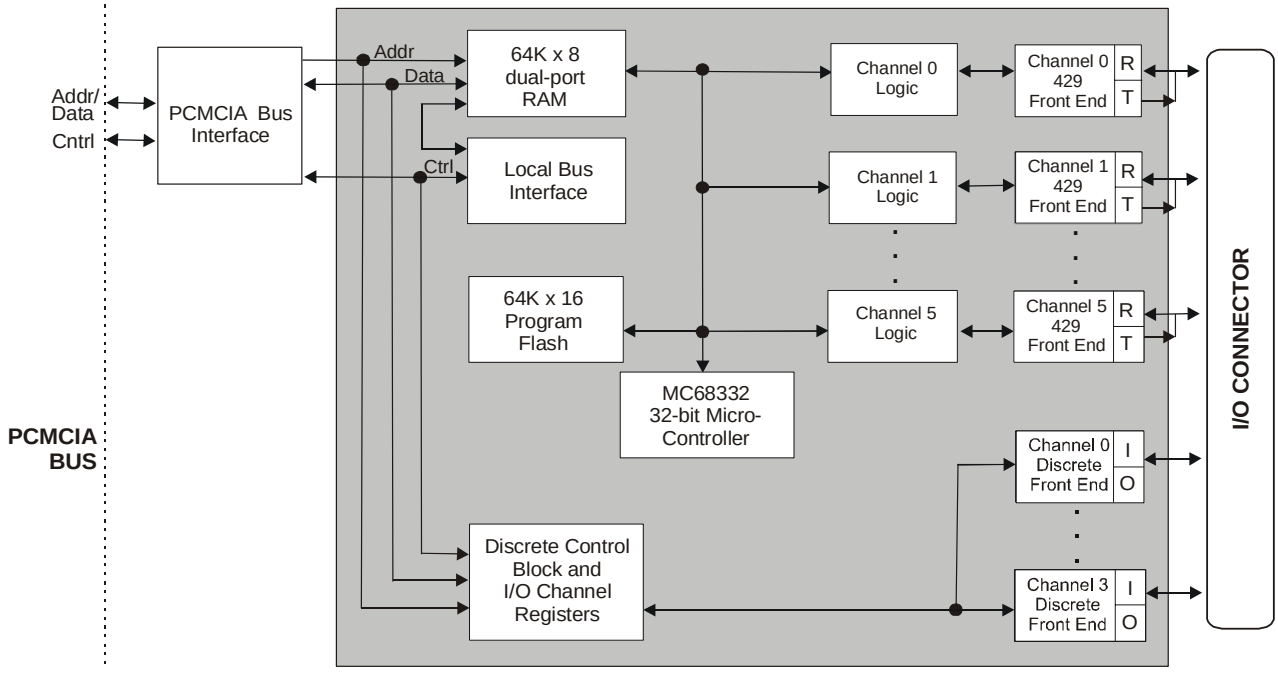

Figure 1-2 DAS-429PCMCIA/RT6D4 Block Diagram

1.2 Installation

For hardware and software installation instructions, see the **readme.pdf** file on the root folder of the installation CD. When downloading new software from the Excalibur website, the **readme.pdf** file is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see the **readme.pdf** file. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, see the Technical Support section of our website: www.mil-1553.com. You can also contact us by phone. To find the location nearest you, see the Contact section of our website.

2 PCMCIA Bus Interface

Chapter 2 describes the PCMCIA bus interface. The following topics are covered:

2.1 Attribute Memory Map 2-2
2.1.1 Card Information Structure (CIS) 2-2
2.1.2 Function Configuration Registers. 2-6
2.2 Common Memory Map 2-7

The PCMCIA standard defines the electrical and physical interface between the PC Card and the host computer, including the 68-pin connector. Detailed specifications can be found in the PCMCIA PC Card Standard.

The *DAS-429PCMCIA/RT[D]* supports two types of address spaces:

- **Attribute Memory Address** space, for the Card Information Structure (CIS) and the Function Configuration Registers.
- **Common Memory Address** space, for regular memory accesses. The dual-port RAM and the Time Tag counter are located in Common Memory.

The Attribute Memory space is selected by driving the signal REG# low, and the Common Memory space is selected by driving the signal REG# high (see Tables 2-1 and 2-2 for details regarding memory access).

FUNCTION	REG#	CE2#	CE1#	A0	OE#	WE#	D15-D8	D7-D0
Standby	X	H	H	X	X	X	Hi-Z	Hi-Z
Lo Byte Read	H	H	L	L	L	H	Hi-Z	Even-Byte
Lo Byte Write	H	H	L	L	H	L	Hi-Z	Even-Byte
Hi Byte Read	H	L	H	X	L	H	Odd-Byte	Hi-Z
Hi Byte Write	H	L	H	X	H	L	Odd-Byte	Hi-Z
Word Read	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write	H	L	L	X	H	L	Odd-Byte	Even-Byte

Table 2-1 Common Memory Access for *DAS-429PCMCIA/RT[D]*

FUNCTION	REG#	CE2#	CE1#	A0	OE#	WE#	D15-D8	D7-D0
Standby	X	H	H	X	X	X	Hi-Z	Hi-Z
Lo Byte Read	L	H	L	L	L	H	Hi-Z	Even-Byte
Lo Byte Write	L	H	L	L	H	L	Hi-Z	Even-Byte
Hi Byte Read	L	L	H	X	L	H	Invalid	Hi-Z
Hi Byte Write	L	L	H	X	H	L	Invalid	Hi-Z
Word Read	L	L	L	X	L	H	Invalid	Even-Byte
Word Write	L	L	L	X	H	L	Invalid	Even-Byte

Table 2-2 Attribute Memory Access for *DAS-429PCMCIA/RT[D]*

Information concerning the format of the card is stored in the Card Information Structure (CIS). The CIS is a variable-length, linked-list of data blocks, called **tuples**. The CIS resides in even bytes of the Attribute Memory, beginning at address 0. Two function configuration registers are located in the Attribute Memory. The configuration registers are repeated in the Common Memory. These allow the user to reset the *DAS-429PCMCIA/RT[D]* card, service interrupts, etc.

2.1 Attribute Memory Map

The Attribute Memory is selected during an even-byte or word access when the host drives the signal REG# low. The Attribute Memory contains the CIS and two Function Configuration Registers. The CIS is read-only. The CIS resides in the even-bytes starting at address 0 and ending when the End of List tuple is encountered. The two Function Configuration Registers are located at addresses 40000 (H) and 40002 (H). The region above the CIS and the Function Configuration Registers is reserved and should not be accessed.

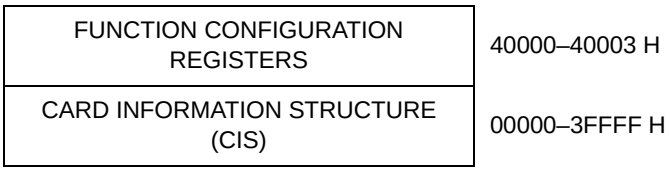

Figure 2-1 Attribute Memory Map

2.1.1 Card Information Structure (CIS)

The Card Information Structure (CIS) contains information about the type of PC card (memory or I/O), the types and sizes of memory, and the interface to the host. Information is stored in a variable-length linked-list of data blocks, called **tuples**. The first byte of each tuple contains the tuple code, which defines what type of information the tuple provides. The next byte is the link byte, which indicates how many bytes remain in the current tuple.

2.1.1.1 Device Tuple for Common Memory

The first tuple identifies the card as a 5V PCMCIA card.

2.1.1.2 Level 1 Version/Product Information Tuple

This tuple contains Level-1-version compliance information as defined in PCMCIA Release 2.0, and information about the card manufacturer. Included are the major version number and the minor version number, 04 (H) and 01 (H) respectively, according to PCMCIA Release 2.0. Also included are the manufacturer name and the product name.

2.1.1.3 Manufacture Identification Tuple

This tuple contains Excalibur System's Manufacturer Code, which is 0145 (H). Also included is the current revision of the CIS table. The revision of the CIS is read as hex numbers. For example, revision 1.0 would be read as 10 (H).

2.1.1.4 Configuration Tuple

This tuple establishes the number and address of the Function Configuration Registers, and indicates the index of the last Configuration Entry Tuple. The *DAS-429PCMCIA/RT[D]* has two Configuration Registers at base address 40000 (H). The index of the last Configuration Entry Tuple is 2.

2.1.1.5 Configuration Entry Tuple

This tuple describes the type of interface utilized by the *DAS-429PCMCIA/RT[D]*.

- Under Windows 9x/ME/2000/XP: from the **`inf`** file on the Excalibur Installation CD.
- Windows NT4: from a registry entry written by the Excalibur Configuration Utility (**`ExcConfig.exe`**)

For more information about the accompanying drivers, see *429RTx Software Tools: Programmer's Reference*.

2.1.1.6 No Link Tuple

This tuple indicates that the CIS doesn't continue in another linked list after the End of List tuple.

2.1.1.7 End of List Tuple

This tuple indicates the end of the linked list.

2.1.1.8 CIS Table

Tuple Addr.	Tuple Value	Tuple Field Name	General Description
00 H	01 H	TPL_CODE	CISTPL_DEVICE
02 H	01 H	TPL_LNK	
04 H	FF H	End of Tuple	
06 H	15 H	TPL_CODE	CISTPL_VERS_1
08 H	2C H	TPL_LNK	
0A H	04 H	TPLLV1_MAJOR	Major version number (04 H)
0C H	01 H	TPLLV1_MINOR	Minor version number (01 H)
0E H	45 H	”E”	Name Of Manufacturer
10 H	78 H	”x”	
12 H	63 H	”c”	
14 H	61 H	“a”	
16 H	6C H	“l”	
18 H	69 H	“i”	
1A H	62 H	“b”	
1C H	75 H	“u”	
1E H	72 H	“r”	
20 H	20 H	“space”	
22 H	53 H	“S”	
24 H	79 H	“y”	
26 H	73 H	“s”	
28 H	74 H	“t”	
2A H	65 H	“e”	
2C H	6D H	“m”	
2E H	73 H	“s”	
30 H	20 H	“space”	
32 H	49 H	“I”	
34 H	6E H	“n”	
36 H	63 H	“c”	
48 H	2E H	“.”	
3A H	00 H	“terminator”	
3C H	44 H	“D”	Name of Product
3E H	41 H	“A”	
40 H	53 H	“S”	
42 H	2D H	“-”	
44 H	34 H	“4”	
46 H	32 H	“2”	
48 H	39 H	“9”	
4A H	50 H	“P”	
4C H	43 H	“C”	
4E H	40 H	“M”	
50 H	43 H	“C”	
52 H	49 H	“I”	
54 H	41 H	“A”	
56 H	2F H	“/”	
58 H	52 H	“R”	
5A H	54 H	“T”	
5C H	44 H	“D”	
5E H	00 H	“terminator”	
60 H	FF H	End of Tuple	

CIS Table

Tuple Addr.	Tuple Value	Tuple Field Name	General Description
62 H	20 H	TPL_CODE	CISTPL_MANFID
64 H	04 H	TPL_LNK	
66 H	45 H	TPLMID_MANF	Manufacturer code for Excalibur Systems Lo
68 H	01 H	TPLMID_MANF	Manufacturer code for Excalibur Systems Hi
6A H	00 H	Reserved	
6C H	***	CIS Revision	*** Revision of CIS (Rev. 1.0 is read as 10 H)
6E H	1A H	TPL_CODE	CISTPL_CONFIG
70 H	06 H	TPL_LNK	
72 H	02 H	TPCC_SZ	3 address bytes for Configuration Registers
74 H	02 H	TPCC_LAST	Index number of last entry is 2
76 H	00 H	TPCC_RADR	Configuration Registers Base Address Lo
78 H	00 H	TPCC_RADR	Configuration Registers Base Address Mid
7A H	04 H	TPCC_RADR	Configuration Registers Base Address Hi
7C H	03 H	TPCC_RMSK	First two Configuration Registers
7E H	1B H	TPL_CODE	CISTPL_CFTABLE_ENTRY
80 H	0C H	TPL_LNK	
82 H	C2 H	TPCE_INDX	Interface follows, Set Default, Index is 2
84 H	80 H	TPCE_IF	WAIT, No Rdy/Bsy, WP, BVD, Memory Type Interface
86 H	61 H	TPCE_FS	VCC required
88 H	01 H	TPCE_PD	VCC: Nominal voltage
8A H	55 H	TPCE_PD	VCC: 5V
8C H	49 H	TPCE_MS	2bytes address size, 1byte length, 2 window descr.
8E H	80 H	TPCE_MS	Window 1 length size = 32K
90 H	00 H	TPCE_MS	Window 1 address size = 000 000 H
92 H	00 H	TPCE_MS	
94 H	01 H	TPCE_MS	Window 2 length size = ¼K
96 H	00 H	TPCE_MS	Window 2 address size 040000 H
98 H	04 H	TPCE_MS	
9A H	14 H	TPL_CODE	CISTPL_NO_LINK
9C H	00 H	TPL_LNK	
9E H	FF H	TPL_CODE	CISTPL_END

CIS Table (cont.)

2.1.2 Function Configuration Registers

The two function configuration registers allow the user to reset the *DAS-429PCMCIA/RT[D]* card, service interrupts, etc. These registers are repeated in the Common memory address 10000 (H) and 10002 (H).

2.1.2.1 Configuration Option Register

Address: 40000 (H)
Read/Write

Bit	Bit Name	Description
07	**Software Reset**	1 = Resets the *DAS-429PCMCIA/RT[D]*. This bit remains high, and the card remains in reset mode, until a 0 is written to this bit. The default value of the reset bit is 1. **Note:** The reset erases all memory locations in the dual-port RAM. The Card Status, Card ID, Firmware Revision registers and location 40002 H are overwritten by the card after the reset operation has been completed.
06	**Reserved**	Set to 1 on read – Ignore on write.
05	**Time Tag Reset**	1 = Resets the Time Tag counter. This bit remains high, and the counter remains in reset mode, until a 0 is written to this bit. The default value of the reset bit is 0.
00-04	**Reserved**	Set to 0 on write. Ignore on read.

Configuration Option Register

2.1.2.2 Configuration & Status Register

Address: 40002 (H)
Read/Write

Bit	Bit Name	Description
02-07	**Reserved**	Set to 0 on write. Ignore on read.
01	**Interrupt Pending**	1 = The *DAS-429PCMCIA/RT[D]* has an interrupt waiting to be serviced. This bit remains high, and the card remains in interrupt pending mode, until a 0 is written to this bit. Writing a 1 to this bit has no effect on the value of the bit. The default value of the interrupt pending bit is 0.
00	**Reserved**	Set to 0 on write. Ignore on read.

Configuration & Status Register

2.2 Common Memory Map

The card takes 68 Kbytes of Common Memory which are shared between the:

- Data memory block
- Channel Control Registers
- Global Control Registers

DAS-429PCMCIA/RT10		DAS-429PCMCIART6D4
Transmit Instruction Stack Transmit Data Blocks Receive Data Blocks Receive Look-Up Tables	00000 – 0F9FF H	Transmit Instruction Stack Transmit Data Blocks Receive Data Blocks Receive Look-Up Tables
Reserved	0FA00 – 0FD1F H	Reserved
Channel Control Register Block 0	0FD20 – 0FD4E H	Channel Control Register Block 0
Channel Control Register Block 1	0FD50 – 0FD0FE H	Channel Control Register Block 1
Channel Control Register Block 2	0FD80 – 0FDAE H	Channel Control Register Block 2
Channel Control Register Block 3	0FDB0 – 0FDDE H	Channel Control Register Block 3
Channel Control Register Block 4	0FDE0 – 0FE0E H	Channel Control Register Block 4
Channel Control Register Block 5	0FE10 – 0FE3E H	Channel Control Register Block 5
Channel Control Register Block 6	0FE40 – 0FE6E H	Reserved
Channel Control Register Block 7	0FE70 – 0FE9E H	
Channel Control Register Block 8	0FEA0 – 0FECE H	
Channel Control Register Block 9	0FED0 – 0FEFE H	
Global Control Registers	0FF00 – 0FF9F H	Global Control Registers
Global Reserved	0FFA0 – 0FFBA H	4 Discrete Channel Control Registers
Card Type Register	FFBC H	Card Type Register
Global Reserved	0FFBE – 0FFFF H	Global Reserved
Configuration Option Register	10000 H	Configuration Option Register
Configuration & Status Register	10002 H	Configuration & Status Register
Reserved Memory Space	10004 – 11000 H	Reserved Memory Space

Figure 2-2 Common Memory Map

For descriptions of the receive and transmit Channel Control Registers and the Global Control Registers, see **Chapter 3: Getting Started**. See **Chapter 5: DAS-429PCMCIA/RT6D4 Operation & Control Registers** for descriptions of the Discrete Control Registers.

3 Getting Started

Chapter 3 provides an overview of ARINC 429 channel operation.

The card operation makes extensive use of pointers for setting up the size and location on both the receiver and data blocks, transmitter instruction stacks and receiver Look-up Tables. Each channel has its own pointer registers so that the unique memory areas may be allocated for each channel. It is also possible to share memory areas. For example, more than one receiver channel may point to and use the same Label Look-up Table that controls which labels will be stored by the card.

The flowchart **Figure 3-1 Card Operation Flowchart** on page 3-2, describes the necessary steps to set up transmit and receive channels. For details how to operate each specific protocol, see the sections: **4.3 Transmit Channel Operation** on page 4-17 and **4.4 Receive Channel Operation** on page 4-22.

After power-up, perform the following steps:

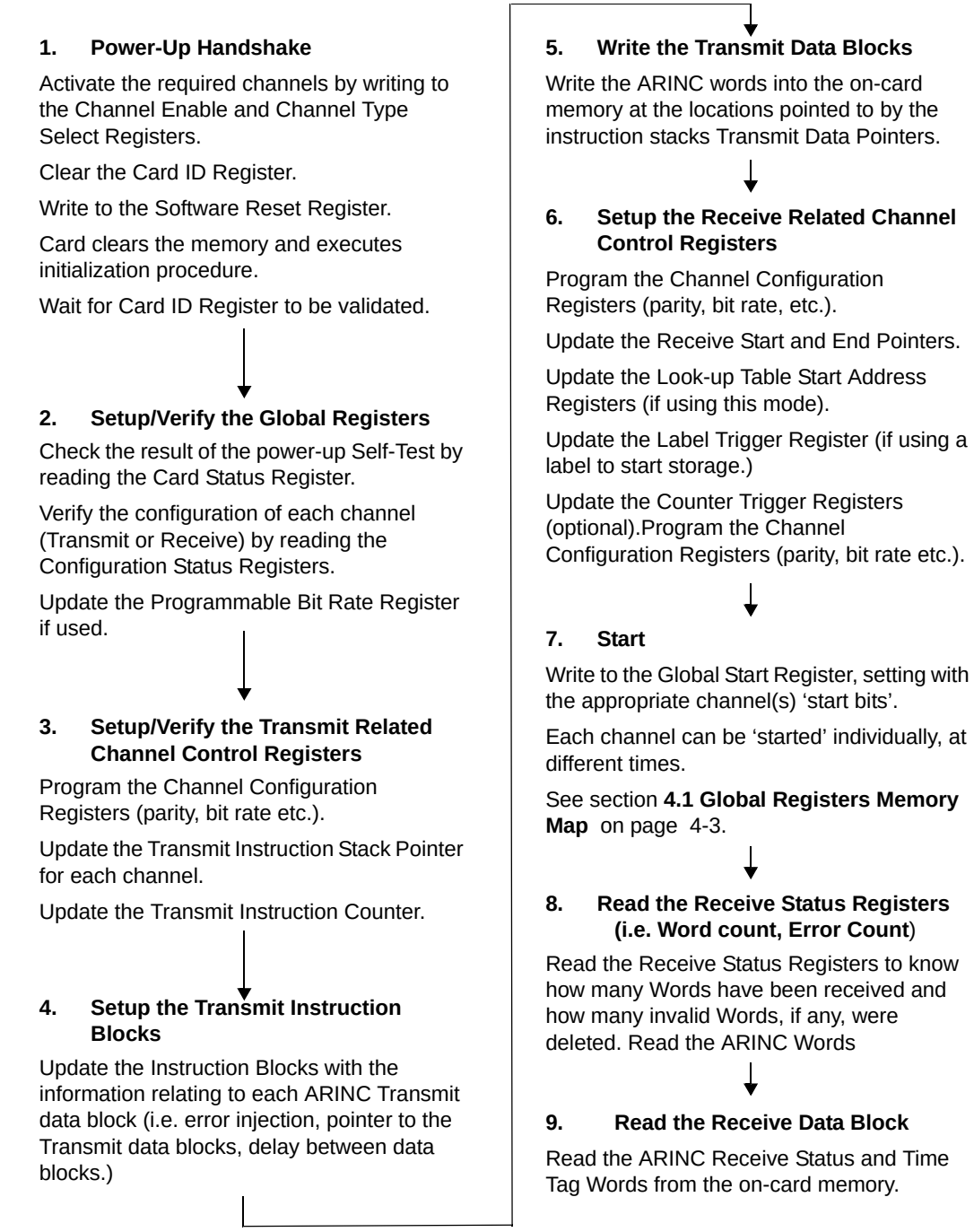
1. Power-Up Handshake
Activate the required channels by writing to the Channel Enable and Channel Type Select Registers.
Clear the Card ID Register.
Write to the Software Reset Register.
Card clears the memory and executes initialization procedure.
Wait for Card ID Register to be validated.
2. Setup/Verify the Global Registers
Check the result of the power-up Self-Test by reading the Card Status Register.
Verify the configuration of each channel (Transmit or Receive) by reading the Configuration Status Registers.
Update the Programmable Bit Rate Register if used.
3. Setup/Verify the Transmit Related Channel Control Registers
Program the Channel Configuration Registers (parity, bit rate etc.).
Update the Transmit Instruction Stack Pointer for each channel.
Update the Transmit Instruction Counter.
4. Setup the Transmit Instruction Blocks
Update the Instruction Blocks with the information relating to each ARINC Transmit data block (i.e. error injection, pointer to the Transmit data blocks, delay between data blocks.)
5. Write the Transmit Data Blocks
Write the ARINC words into the on-card memory at the locations pointed to by the instruction stacks Transmit Data Pointers.
6. Setup the Receive Related Channel Control Registers
Program the Channel Configuration Registers (parity, bit rate, etc.).
Update the Receive Start and End Pointers.
Update the Look-up Table Start Address Registers (if using this mode).
Update the Label Trigger Register (if using a label to start storage.)
Update the Counter Trigger Registers (optional).Program the Channel Configuration Registers (parity, bit rate etc.).
7. Start
Write to the Global Start Register, setting with the appropriate channel(s) 'start bits'.
Each channel can be 'started' individually, at different times.
See section 4.1 Global Registers Memory Map on page 4-3.
8. Read the Receive Status Registers (i.e. Word count, Error Count)
Read the Receive Status Registers to know how many Words have been received and how many invalid Words, if any, were deleted. Read the ARINC Words
9. Read the Receive Data Block
Read the ARINC Receive Status and Time Tag Words from the on-card memory.

Figure 3-1 Card Operation Flowchart

4 Card Operation

Chapter 4 describes *DAS-429PCMCIA/RT[D]* card operation.

Note: References to channels 5 – 9 are *only* for the *DAS-429PCMCIA/RT10*. For the Discrete channels on the *DAS-429PCMCIA/RT6D4*, which replace channels 5–9, see **Chapter 5: DAS-429PCMCIA/RT6D4 Operation & Control Registers**.

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4.1 Global Registers Memory Map

The Global Registers can be set at any time.

Reserved	0FF00–0FF3A H	Channel 8 Configuration Status	0FF6A H
		Channel 9 Configuration Status	0FF6C H
Interrupt Status Busy	0FF3C H	Programmable Bit Rate	0FF6E H
Receive Merge Status	0FF3E H	Interrupt Status	0FF70 H
Receive Merge Interrupt/Trigger Condition	0FF40 H	Firmware Revision	0FF72 H
Receive Merge Configuration	0FF42 H	Card Status	0FF74 H
Receive Merge Label Trigger	0FF44 H	Card ID	0FF76 H
Receive Merge Error Count	0FF46 H	Reserved	0FF78 H
Receive Merge Interval Count Trigger	0FF48 H	Start / Stop	0FF7A H
Receive Merge Buffer Wraparound	0FF4A H	Time Tag Reset	0FF7C H
Receive Merge Word Count Trigger	0FF4C H	Reserved	0FF7E – 0FF82 H
Receive Merge Word Count	0FF4E H		
Receive Merge Filter Table Start Address	0FF50 H	Software Reset	0FF84 H
Receive Merge Current Pointer	0FF52 H	Reserved	0FF86 – 0FF8E H
Receive Merge End Pointer	0FF54 H		
Receive Merge Start Pointer	0FF56 H	Time Tag Counter	0FF90 – 0FF92 H
Receive Data Storage Mode	0FF58 H	Hardware Revision	0FF94 H
Channel 0 Configuration Status	0FF5A H	Reserved	0FF96 H
Channel 1 Configuration Status	0FF5C H	Channel Enable	0FF98 H
Channel 2 Configuration Status	0FF5E H	Channel Type Select	0FF9A H
Channel 3 Configuration Status	0FF60 H	Reserved	0FF9C– 0FFBA H
Channel 4 Configuration Status	0FF62 H	Card Type Register	0FFBC H
Channel 5 Configuration Status	0FF64 H	Reserved	0FFBE – 0FFFF H
Channel 6 Configuration Status	0FF66 H	Configuration Option Register	10000 H
Channel 7 Configuration Status	0FF68 H	Configuration & Status Register	10002 H

Figure 4-1 Global Registers Memory Map

4.2 Global Register Definitions

4.2.1 Interrupt Status Busy Register

Address: 0FF3C (H)

The Interrupt Status Busy Register indicates if the Channel *x* Status Register, the Receive Merge Status Register and the Interrupts Status Register may be accessed by the user.

Bit	Bit Name	Description
11-15		Reserved
10	**MRGBSY**	1 = Receive Merge Status Register is busy – do not access the register 0 = The contents of the register is valid and may be accessed
09	**CH9BSY**	1 = Channel 9 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 9 Status Register may be accessed
08	**CH8BSY**	1 = Channel 8 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 8 Status Register may be accessed
07	**CH7BSY**	1 = Channel 7 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 7 Status Register may be accessed
06	**CH6BSY**	1 = Channel 6 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 6 Status Register may be accessed
05	**CH5BSY**	1 = Channel 5 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 5 Status Register may be accessed
04	**CH4BSY**	1 = Channel 4 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 4 Status Register may be accessed
03	**CH3BSY**	1 = Channel 3 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 3 Status Register may be accessed
02	**CH2BSY**	1 = Channel 2 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 2 Status Register may be accessed
01	**CH1BSY**	1 = Channel 1 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 1 Status Register may be accessed
00	**CH0BSY**	1 = Channel 0 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 0 Status Register may be accessed

Interrupt Status Busy Register

Note: Before accessing the Global Interrupt Register, the user should wait until the Interrupt Status Busy Register = 0. The user then has at least 15 msec. to safely access the status registers.

4.2.2 Receive Merge Status Register

Address: 0FF3E (H)

The Receive Merge Status Register indicates the operational status of the Merge Mode receive buffer. This register can be used to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. Writing a 0 to this register resets the status bits.

Bit	Bit Name — Interrupt Causes
07-15	Reserved
06	Stopped on Buffer Full
05	Error Word Received
04	Word Count Trigger
03	Interval Count Trigger
02	Label Received
00-01	Reserved

Receive Merge Status Register

Note: The Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the Filter Table.

4.2.3 Receive Merge Interrupt/Trigger Condition Register

Address: 0FF40 (H)

The Receive Merge Interrupt/Trigger Condition Register sets the Interrupt and Trigger condition or conditions for receive channels in Merge Mode. The Trigger Conditions set a pulse on the External Trigger Output.

Note: The Trigger Condition Bits are only relevant to the -002 card, which supports External Trigger Output. For more information about this card, contact Customer Service.

Trigger Condition Bits 08 – 15		Interrupt Condition Bits 00 – 07	
Bit	**Bit Name**	**Bit**	**Bit Name**
15	Reserved	**07**	Reserved
14	Stopped on buffer full	**06**	Stopped on buffer full
13	Error Word received	**05**	Error Word received
12	Data Word Count Trigger	**04**	Data Word Count Trigger
11	Interval Count Trigger	**03**	Interval Count Trigger
10	Label Received	**02**	Label Received
08–09	Reserved	**00–01**	Reserved

Receive Merge Interval/Trigger Condition Register

Note:
1. The Label Received interrupt or trigger only occurs upon reception of a label that has been marked for interrupt in the Filter Table.
2. To activate the Interval Count Trigger interrupt or trigger, the Receive Merge Interval Count Trigger Register must also be set. (see **Receive Merge Interval Count Trigger Register** on page 4-7).

3. To activate Data Word Count Trigger interrupt or trigger, the Receive Merge Word Count Trigger Register must also be set. (see **Receive Merge Word Count Trigger Register** on page 4-7).

4.2.4 Receive Merge Configuration Register

Address: 0FF42 (H)

The Receive Merge Configuration Register sets up run parameters for Merge Mode.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**Enable Receive Filter Table**	1 = Enable filter table. (Stores Labels per table 0 = Disables table. Stores all Labels.
08	**Reserved**	Set to 0
07	**Receive Label Trigger**	1 = Start data storage upon receipt of Label *xx*. (see Receive Merge Label Trigger Register) 0 = Receive stores data without Start Label Trigger.
06	**Receive Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receive wraps around the data in the block.
00-05	**Reserved**	Set to 0

Receive Merge Configuration Register

4.2.5 Receive Merge Label Trigger Register

Address: 0FF44 (H)

The Receive Merge Label Trigger Register is used in conjunction with the Receive Label Trigger bit in the Receive Merge Configuration Register to begin the reception and storage of data upon receipt of a unique ARINC label.

The card will not store any ARINC words received prior to the first instance of this label.

Bit	Description
08–15	Set to 0
00–07	Trigger Label

Receive Merge Label Trigger Register

4.2.6 Receive Merge Error Count Register

Address: 0FF46 (H)

The Receive Merge Error Count Register is a 16-bit counter. The register indicates the number of error words received on the channel. This counter Register wraps around and is reset only by the user.

4.2.7 Receive Merge Interval Count Trigger Register

Address: 0FF48 (H)

The Receive Merge Interval Count Trigger Register (a 16-bit value) allows the user to generate an interrupt (or pollable bit) every *N* number of words, where *N* is the value written to this register. For example, to request an interrupt after every five ARINC words, write 05 to this register.

To generate an interrupt or trigger, the appropriate bit must also be set in the Receive Merge Interrupt Condition Register (see **Receive Merge Interrupt/Trigger Condition Register** on page 4-5).

4.2.8 Receive Merge Buffer Wraparound Register

Address: 0FF4A (H)

The Receive Merge Buffer Wraparound Register contains 2 bits for synchronization with the host.

Bit	Description
15	Multiple Wraparound - data lost
14	Single Wraparound - the receive buffer has wrapped around once since the last data read
00–13	Reserved

Receive Merge Buffer Wraparound Register

4.2.9 Receive Merge Word Count Trigger Register

Address: 0FF4C (H)

The Receive Merge Word Count Trigger Register sets a trigger (used for polling or interrupts) and a flag that indicates when a specific number of words have been received (1 - 65535).

To generate a trigger or interrupt, the appropriate bit in the Receive Merge Interrupt/ Trigger Condition Register must also be set. (see **Receive Merge Interrupt/ Trigger Condition Register** on page 4-5).

Note: This trigger is set when the value in the Receive Merge Word Counter matches the value set in this register.

4.2.10 Receive Merge Word Counter

Address: 0FF4E (H)

The Receive Merge Word Counter indicates the number of ARINC words received (0 - 65535). This register wraps around to 0 after it reaches 65535. The user can reset the register only when the channel is stopped.

4.2.11 Receive Merge Filter Table Start Address

Address: 0FF50 (H)

The Receive Merge Filter Table Start Address sets the start address of the (256×8) Label Filter Table as described in the Sequential storage mode (see **Receive Buffer Storage Sequence** on page 4-23.) The address must be on a word boundary.

4.2.12 Receive Merge Current Pointer

Address: 0FF52 (H)

The Receive Merge Current Pointer indicates the current address where the next ARINC receive word is to be placed in the Receive buffer. This pointer value is incremented after the entire receive block (ARINC word, Time Tag, and Status) is written into memory.

4.2.13 Receive Merge End Pointer

Address: 0FF54 (H)

The Receive Merge End Pointer sets the End Address of the Receive Data buffer. The data will wrap around or stop when the buffer is full, (when the End Address is reached), depending upon the contents of the Receive Merge Configuration Register Wraparound bit. (See **Receive Merge Configuration Register** on page 4-6).

4.2.14 Receive Merge Start Pointer

Address: 0FF56 (H)

The Receive Merge Start Pointer sets the Start Address of the Receive Data buffer. The address must be on a word boundary within the Receive Data Blocks area.

Example: To cause the Merge buffer to begin at byte offset 001A0 (H), write a 01A0 (H) to this register.

4.2.15 Receive Data Storage Mode Register

Address: 0FF58 (H)

The Receive Data Storage Mode register is used to select the Receive Data Storage Mode and the Merge Mode option. ARINC Data Words can be stored with, or without, Time Tag and Status words appended to the data block. The Merge Mode Control Registers are used only when the Merge Mode option is selected.

Bit	Bit Name	Description
02-15	Reserved – set to 0	
01	Merge Mode option	0 = Independent Mode – utilizes different receive buffer areas for each receive channel. 1 = Merge Mode – each Receive Status Word is tagged with Channel Code information.
00	Data Only Storage Mode option	0 = Standard Mode – appends both Time Tag and Status Words to each ARINC word stored in memory 1 = Store Only Data

Receive Data Storage Mode Register

Note:
1. If Data Only Storage Mode is selected (bit 00 set to 1), storage will be per independent channel regardless of the state of bit 01.
2. Data Only Storage Mode is not available in Look-up Table Mode.
3. The Receive Data Storage Mode Register can only be changed when all the channels are turned off for at least 1 msec. (Start/Stop register = 0).

4.2.16 Channel *x* Configuration Status Register

Address: 0FF5A – 0FF6C (H)

These Registers indicate to the host the type of channel configured in each channel socket on the card.

Bit	Description				
04-15	Reserved – set to 0				
00-03	Configuration Status Code				
	Bit 3	Bit 2	Bit 1	Bit 0	Configuration Status Code
	0	0	0	0	Undefined Channel
	0	0	0	1	ARINC-429 Receive Channel
	0	0	1	0	ARINC-429 Transmit Channel

Channel *x* Configuration Status Register

4.2.17 Programmable Bit Rate Register

Address: 0FF6E (H)

The Programmable Bit Rate Register selects the programmable bit rate value for the ARINC channels. This register is only read by the firmware when the Start/ Stop Register contains a value of 0, i.e. all channels are inactive for at least 1 msec.

Bit	Description
15	Set this bit to 1 (to be the same as Bit 12 of the Card Status Register. See **Card Status Register** on page 4-11.)
11-14	Reserved – set to 0
00-10	Bit Rate value

Programmable Bit Rate Register

1. To calculate the Bit Rate Value (BRV)

$$BRV = \frac{5000}{\text{freq (KHz)}} - 1$$

Example: Desired programmable bit rate 12.5 KHz:

$$BRV = \frac{5000}{12.5\text{KHz}} - 1 = 399\text{Dec (018F H)}$$

Write the value 818F (H) to this register.

4.2.18 Interrupt Status Register

Address: 0FF70 (H)

The Interrupt Status Register indicates which channel issued the interrupt: 1 = Active. The status bit or bits are only reset by the user.

Bit	Bit Name
10-15	Reserved – set to 0
09	Channel 9 Interrupt Status Bit
08	Channel 8 Interrupt Status Bit
07	Channel 7 Interrupt Status Bit
06	Channel 6 Interrupt Status Bit
05	Channel 5 Interrupt Status Bit
04	Channel 4 Interrupt Status Bit
03	Channel 3 Interrupt Status Bit
02	Channel 2 Interrupt Status Bit
01	Channel 1 Interrupt Status Bit
00	Channel 0 Interrupt Status Bit

Interrupt Status Register

4.2.19 Firmware Revision Register

Address: 0FF72 (H)

The Firmware Revision Register indicates the revision level of the firmware. For example: 0114 (H) = Rev 1.14.

4.2.20 Card Status Register

Address: 0FF74 (H)

The Card Status Register indicates the result of the power-up, Self-test of the card.

Note: Only enabled channels can pass the Self-test. See **Channel Enable Register** on page 4-14 and **Channel Type Select Register** on page 4-15.

Bit	Bit Name	
14–15	Reserved	Set to 0
13	Extended Time Support	1 = Extended Interblock Time/Data Rate Mode supported 0 = Not supported (See **Interblock Time/Data Rate Word** on page 4-20.)
12	Baud Rate Generator	1 = 40 MHz
11	Host Ready Timeout	
10	Memory Status Bit	1 = Memory OK 0 = Memory failed
09	Channel 9 Status bit	1 = Self-test OK 0 = Self-test failed
08	Channel 8 Status bit	1 = Self-test OK 0 = Self-test failed
07	Channel 7 Status bit	1 = Self-test OK 0 = Self-test failed
06	Channel 6 Status bit	1 = Self-test OK 0 = Self-test failed
05	Channel 5 Status bit	1 = Self-test OK 0 = Self-test failed
04	Channel 4 Status bit	1 = Self-test OK 0 = Self-test failed
03	Channel 3 Status bit	1 = Self-test OK 0 = Self-test failed
02	Channel 2 Status bit	1 = Self-test OK 0 = Self-test failed
01	Channel 1 Status bit	1 = Self-test OK 0 = Self-test failed
00	Channel 0 Status bit	1 = Self-test OK 0 = Self-test failed

Card Status Register

Note: The card continues to operate on condition of channel Self-test failure, but will *not* operate on condition of memory failure.

4.2.21 Card ID Register

Address: 0FF76 (H)

The Card ID register indicates that the card has completed its initialization sequence and that the card is ready to be accessed by the host. The card writes the value A429 (H) into this register when ready.

4.2.22 Start/Stop Register

Address: 0FF7A (H)

The user can start one or more channels at the same time — wait a minimum of 500 μsec. between writes to this register.

Bit	Description	
10-15	Reserved – set to 0	
09	Channel 9 Start Bit	1 = Start 0 = Stop
08	Channel 8 Start Bit	1 = Start 0 = Stop
07	Channel 7 Start Bit	1 = Start 0 = Stop
06	Channel 6 Start Bit	1 = Start 0 = Stop
05	Channel 5 Start Bit	1 = Start 0 = Stop
04	Channel 4 Start Bit	1 = Start 0 = Stop
03	Channel 3 Start Bit	1 = Start 0 = Stop
02	Channel 2 Start Bit	1 = Start 0 = Stop
01	Channel 1 Start Bit	1 = Start 0 = Stop
00	Channel 0 Start Bit	1 = Start 0 = Stop

Start/Stop Register

Note: Only after the Start/Stop Register contains a 0 for at least 1 msec. do any changes in a channel's Configuration, Programmable Bit Rate , or Receive Data Storage Mode Registers take effect on the card.

4.2.23 Time Tag Reset Register

Address: 0FF7C (H)

Write Writing any value to the Time Tag Reset Register causes the Time Tag to be reset to 0.

4.2.24 Software Reset Register — Address: 0FF84 (H)

Write Writing a 0 to the Software Reset Register resets the card. Following a reset, the card executes a Self-test, both memory and channels, clears all the dual-port RAM, resets the card's interrupts and updates the Card Status Register. The card then indicates that it is ready by writing a value of A429 (H) to the Card ID Register.

4.2.25 Time Tag Counter — Address: 0FF90–0FF92 (H)

The two Time Tag Counter Words represent the current value of the free-running 32-bit Time Tag counter. The counter can be read at any time. The following sequence must be kept:

First: 0FF90 H (Lo word – LSB)
Last: 0FF92 H (Hi word – MSB)

The resolution of the counter is 10 μsec. The counter is reset to 0 upon power-up or software rest or through the Time Tag Reset register. After the reset operation, the counter starts counting. When the counter reaches the value FFFF FFFF (H), it wraps around to 0 and continues counting.

4.2.26 Hardware Revision Register — Address: 0FF94 (H)

Read The Hardware Revision register indicates the card type and the revision level of each part of the hardware.

Bit	Description		
12-15	**Card type**	A = *RT[D]*	
8-11	**FPGA Rev.**	1 = Rev1 2 = Rev2 • • • 9 = Rev9	Revision of the 429 interface block
00-07	**Reserved**		

Hardware Revision Register

4.2.27 Channel Enable Register

Address: 0FF98 (H)

Write

The Channel Enable register is used to enable/activate the required channels. This register, in conjunction with the Channel Type Select register, must be set first, before any other operations are carried out on the card. This register is reset to 0000 after card reset.

Note: In order for the on-card micro controller to recognize the channel's definitions, a software reset has to be applied. (See **Software Reset Register** on page 4-13.)

Bit	Description	
10-15	Reserved – set to 0	
09	Channel 9 enable bit	1 = enabled 0 = disabled
08	Channel 8 enable bit	1 = enabled 0 = disabled
07	Channel 7 enable bit	1 = enabled 0 = disabled
06	Channel 6 enable bit	1 = enabled 0 = disabled
05	Channel 5 enable bit	1 = enabled 0 = disabled
04	Channel 4 enable bit	1 = enabled 0 = disabled
03	Channel 3 enable bit	1 = enabled 0 = disabled
02	Channel 2 enable bit	1 = enabled 0 = disabled
01	Channel 1 enable bit	1 = enabled 0 = disabled
00	Channel 0 enable bit	1 = enabled 0 = disabled

Channel Enable Register

4.2.28 Channel Type Select Register

Address: 0FF9A (H)

Write

The Channel Type Select Register sets each channel's type, either transmit or receive. This register, in conjunction with the Channel Enable Register, must be set prior to any other operations are carried out on the card. This register is reset to 0000 after card reset. See **Figure 3-1 Card Operation Flowchart** on page 3-2.

Note: In order for the on-card micro-controller to recognize the channel's definitions, a software reset has to be applied. (See **Software Reset Register** on page 4-13.)

Bit	Description	
06-15	Reserved – set to 0	
05	Channel 5 type select bit	1 = transmit 0 = receive
04	Channel 4 type select bit	1 = transmit 0 = receive
03	Channel 3 type select bit	1 = transmit 0 = receive
02	Channel 2 type select bit	1 = transmit 0 = receive
01	Channel 1 type select bit	1 = transmit 0 = receive
00	Channel 0 type select bit	1 = transmit 0 = receive

Channel Type Select Register

4.2.29 Card Type Register

Address: 0FFBC (H)

Read

The Card Type registers shows the card configuration.

Bit	Bit Name	
04–15	**Reserved**	
00–03	**Card type**	A = DAS-429PCMCIA/RT10
		D = DAS-429PCMCIA/RT6D4

Card Type Register

4.2.30 Configuration Option Register **Address: 10000 (H)**

Read/Write The Configuration Option Register is repeated in the Attribute Memory at address 40000 (H).

Bit	Bit Name	Description
07	**Software Reset**	1 = Resets the *DAS-429PCMCIA/RT[D]*. This bit remains high, and the card remains in reset mode, until a 0 is written to this bit. The default value of the reset bit is 1. **Note:** The reset erases all memory locations in the dual-port RAM. The Card status, Card ID, Firmware Revision registers and location 10002 H are overwritten by the card after the reset operation has been completed.
06	**Reserved**	Set to 1 on read Ignore on write.
05	**Time Tag Reset**	1 = Resets the Time Tag counter. This bit remains high, and the counter remains in reset mode, until a 0 is written to this bit. The default value of the reset bit is 0.
00-04	**Reserved**	Set to 0 on write. Ignore on read.

Configuration Option Register

4.2.31 Configuration & Status Register **Address: 10002 (H)**

Read/Write The Configuration & Status Register is repeated in the Attribute Memory at address 40002 (H).

Bit	Bit Name	Description
02-07	**Reserved**	Set to 0 on write. Ignore on read.
01	**Interrupt Pending**	1 = The *DAS-429PCMCIA/RT[D]* has an interrupt waiting to be serviced. This bit remains high, and the card remains in interrupt pending mode, until a 0 is written to this bit. Writing a 1 to this bit has no effect on the value of the bit. The default value of the interrupt pending bit is 0.
00	**Reserved**	Set to 0 on write. Ignore on read.

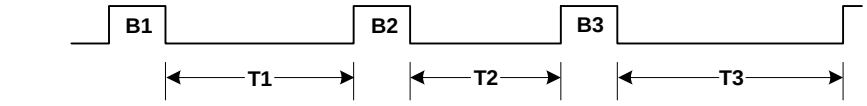
Configuration & Status Register

4.3 Transmit Channel Operation

In transmit channel operation Words are sent out in Blocks (groups of Words). Each Block is sent with dedicated parameters: for example Word count, interblock time, and error injection. The Blocks reside sequentially in stack structure, each pointing to its Data Buffer. The Blocks can be sent either Continuously or *N* times.

Each transmit channel has two basic modes of operation:

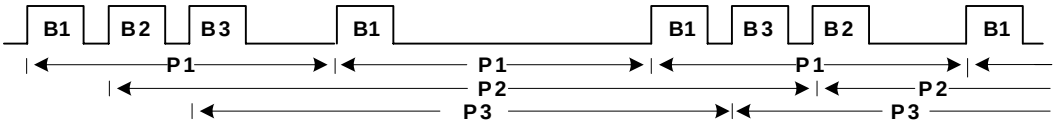
Interblock Time Mode sends out sequential blocks of Words, each followed with its Interblock delay time.



B - Block
T - Interblock time

Figure 4-2 Interblock Time Mode

Data Rate Mode sends out periodically blocks of Words, each with its period (data rate) time.



B - Block
T - Interblock time
P - Block period time

Figure 4-3 Data Rate Mode

In transmit operation the user:

- Sets up the transmitting channel's parameters by writing to the various Channel *x* Control Registers;
- Creates an Instruction Stack for the transmitting channel;
- Writes the data into the dual-port RAM;
- Start transmission by writing to the Start/Stop Register found within the Global Control Register area.

The sequence of writes to memory is not important, except for the write to Start Register operation, which is performed last.

4.3.1 Transmit Instruction Block

The Transmit Instruction Stack is divided into Instruction Blocks, each containing four Words. Each Instruction Block relates to a Data Buffer. A Data Buffer contains one or more ARINC Words which the user desires to transmit with the same amount of delay time between each Word. The stack is sequential, so that the first Instruction Block follows the second Data Block, and so on.

The Instruction Block consists of:

1st Word: The Control Word, which contains error injection parameters.

2nd Word: Contains 2 bytes:

- An 8-bit Word Count which instructs the card as to the number of ARINC Words to transmit within a particular block, and
- An 8-bit, inter-word delay value which programs the time between Words within the same buffer.

3rd Word: Contains a 16-bit, user-supplied data pointer. This is a 16-bit address (must be a Word boundary) that points to the beginning of the Data Words within the memory.

4th Word: Is the Interblock Time/Data Rate value and is used to program the time between Data Block transfers or the transmission period for the specific data block.

Figure 4-4 illustrates the Transmit Instruction Stack structure.

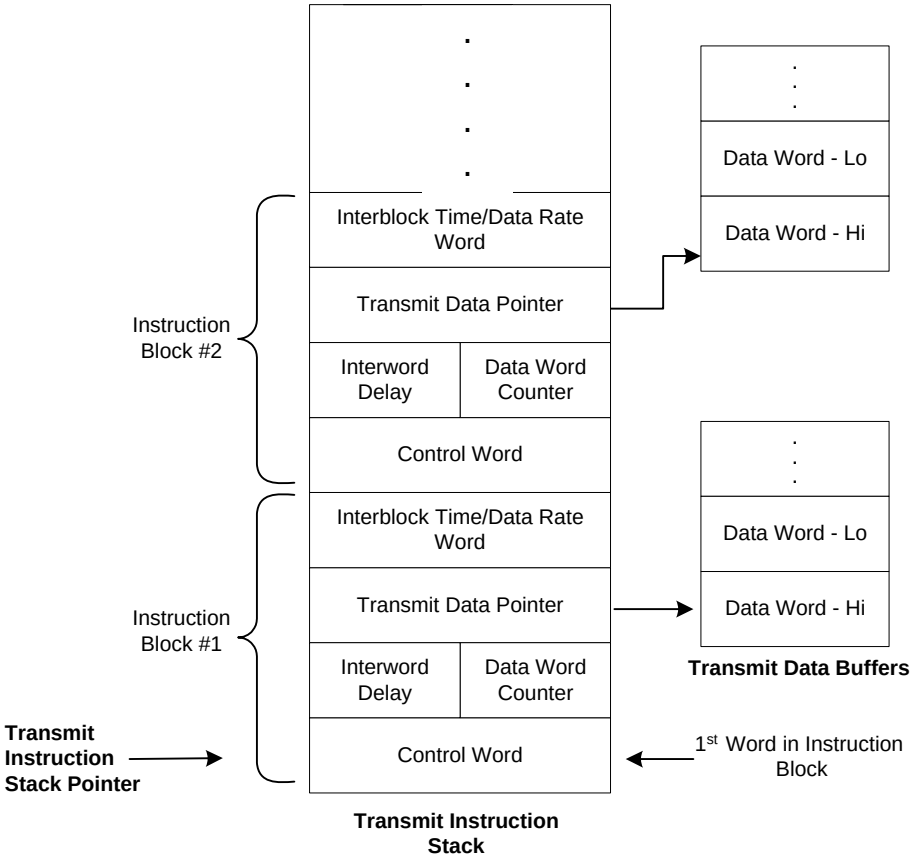


Figure 4-4 Transmit Instruction Stack Structure

CONTROL WORD DEFINITION

This is the 1st Word in the ARINC Transmit Instruction Block.

Bit	Bit Name	Description
06-15	**Reserved**	Set to 0
05	**Suppress Parity** [1]	1 = Forces a no-parity condition within the Word even though 'parity-on' has been selected in the Channel *x* Configuration Register 0 = Regular parity as set up in the Channel *x* Configuration Register
04	**Bit Count Lo Error**	1 = Thirty-one ARINC bits are transmitted within each Word within the block 0 = No error
03	**Bit Count Hi Error**	1 = Thirty-three ARINC bits are transmitted within each Word within the block 0 = No error
02	**Stretch Bit Error**	1 = The 2nd ARINC bit within each Word within the block is 'stretched' causing a Manchester coding error. 0 = No error
01	**Null Bit Error**	1 = A Null Bit Error is inserted within the second bit of each Word within the Block (ARINC Bit 02). 0 = No error
00	**Parity Error**	1 = A Parity Error is inserted within all ARINC Words within the block. 0 = No error

Control Word Definition

1. The **Suppress Parity** is useful when most of the Data Buffers contain standard data with parity and a few buffers contain data type without parity. In such a case, the parity can be set ON for all Words within the Channel x Configuration Register while exceptional cases, can be forced to NO PARITY, using this bit.

INTERWORD DELAY/DATA WORD COUNTER WORD

This Word is divided into two bytes, the Interword Delay (high byte) and the Data Word Counter (low byte).

The Interword Delay byte specifies the time between Words within this data block. The resolution is in the form of 'bit times' according to the transmission bit rate.

Bit Rate	Resolution
Lo-Speed	80μsec/bit
Hi-Speed	10μsec/bit
Programmable	$\frac{1}{\text{Programmable Bit Rate}}$

Interword Delay Resolution

Note: The ARINC specification defines the minimum Interword time as 4 bit times, so values less that 4 may be interpreted on the receiving side as sync error.

The Word Counter byte specifies the number of data Words within this Data block (1-255).

TRANSMIT DATA POINTER

The Transmit Data Pointer is used to set the start address of the block's Transmit Data Buffer. The address must be a Word boundary. The size of the buffer is determined by the Data Word Count value.

INTERBLOCK TIME/DATA RATE WORD

The Interblock Time/Data Rate Word has two functions:

- In **Interblock Time Mode,** the Instruction Blocks are accessed sequentially and their associated Data Words transmitted according to this sequential order. The Interblock Time allows the user to specify the time between Data Blocks. It is inserted after the block transmission.
- In **Data Rate Mode**, the user can specify the transmission period of the particular Data Block. If the number *N* is written to this location, then the message is transmitted every *N* bit times.

The resolution of this 16-bit Word is according to the bit rate selected in the Channel *x* Configuration register, which is the same as the resolution of the Interword Delay byte. (For a detailed explanation of the resolution, see **Interword Delay/Data Word Counter Word** on page 4-19).

The maximum value for the Interblock Time/Data Rate is 65,535 bit times, which is 655 msec. in Hi-speed and 5,243 msec. in Lo-speed. When a longer Interblock Time/Data Rate is required, the user can enable Extended Time Mode. In Extended Time Mode, the actual Interblock Time/Data Rate implemented on the bus will be twice the specified value. (See **Channel x Configuration Register** on page 4-45.)

The transmit mode is set by the Transmit Mode Select bit (bit 08) in the Channel *x* Configuration Register. (See **Channel x Configuration Register** on page 4-45.)

Note: In Data Rate Mode, a scratch buffer for the firmware must be allocated via the **Channel x Scratch Buffer Start Register** and **Channel x Scratch Buffer End Register,** see 4-40.

4.3.2 Transmit Data Block Format

Figure 4-5 **Transmit Data Block**, illustrates the format of the Transmit Data Words within the memory.

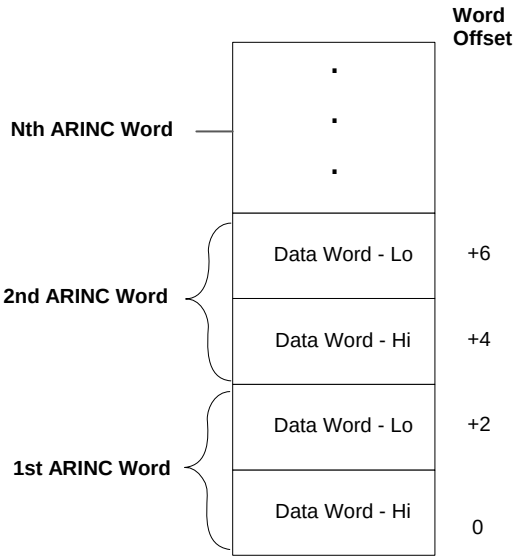


Figure 4-5 Transmit Data Block

Figure 4-6 defines the locations and bit definitions of the data bytes within the memory. The numbers shown in the two Words represent the ARINC Word bit numbers.

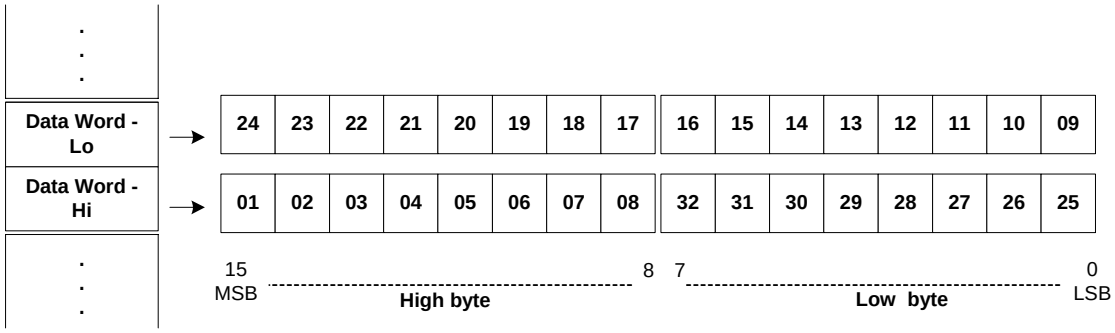


Figure 4-6 32-Bit Transmit Data Words Format

1. The numbers contained within the Words in Figure 4-6 represent the ARINC bit locations within the 32-bit Word.
2. The ARINC Word bits are transmitted in the following order:

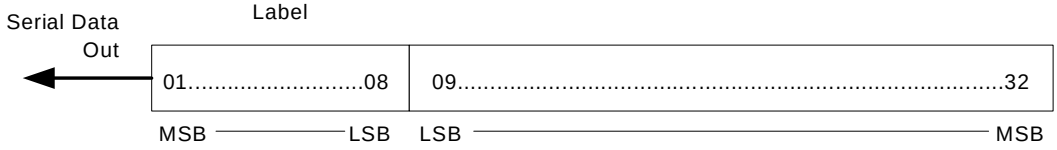


Figure 4-7 32-Bit Word Transmit Order Bit

3. Bits 09 through 32 are ordered from LSB to MSB (as opposed to the Label field that is organized from MSB to LSB). For this reason, in the Data Block, the Hi-Word is first, followed by the Lo-Word, with the Label and the ARINC field 32 through 25 in the Hi-Word and bits 24 through 09, in the Lo-Word.

4.4 Receive Channel Operation

The user sets up each receive channel's mode of operation by writing to various Control Registers (global and channel specific). Each receive channel has three basic modes of operation:

Sequential Mode:	Stores data in sequential locations within the receive data area
Merge Mode:	Siphons all ARINC receive channels data into *one* receive buffer area
Look-Up Table Mode:	Allows the user to store Words in specific locations of memory according to the Label

In all these modes, the Data Words are stored with a 16-bit Receive Status Word and a 32-bit Time Tag value. In Data Only option the Status and Time Tag are not stored. In Merge Mode, the channel ID information (indicates on which channel the data was received) is contained within the Receive Status Word.

In Receive Channel Operation the card is initialized in a wait loop, looking for a START command from the computer. This command is issued by writing to the Global Start Register. (See the **Global Start/Stop Register** on page 4-12). The command instructs the card to begin operation on the selected channels.

4.4.1 Sequential and Merge Modes

Sequential Mode

The Sequential Mode has a software-selectable feature that filters the storage of the specific, user-defined Labels or stores all Labels within a buffer. (See **Figure 4-8 Receive Sequential Mode Buffer Structure** on page 4-23.) The data buffer's size and location within the memory is programmed via a Start and End pointer. (See **Channel x Receive Data Start Pointer** and **Channel x Receive Data End Pointer**, on 4-44). Each received ARINC Data Word is tagged with a status Word, indicating the status of the receive Word and a 32-bit Time Tag value.

These five, 16-bit Words make up a single receive data block. Alternatively, the Sequential Mode offers the user the capability of storing only the ARINC data without the Time Tag and Status Words. This global selection affects all receive channels. (See **Receive Data Storage Mode Register** on page 4-9.) A 16-bit register indicates the number of invalid Words received. Interrupts and pollable status registers allow for numerous event recognition and are described in the Channel Control Register section of this manual. (See **Channel x Configuration Register** on page 4-45).

Merge Mode

The Merge Mode operates in the same manner as the Sequential Mode except that all the receive channels are merged into one Data Buffer area. The Control registers for the Merge Mode are located on the Global Registers Map on 4-3 and defined in section **4.2 Global Register Definitions**.

In this mode the Receive Data Blocks are stored in sequential order and each receive Status Word is tagged with a channel ID, indicating the channel on which the data was received. Each data block contains a Time Tag word as in the standard Sequential Mode of operation.

RECEIVE BUFFER STORAGE SEQUENCE

Figure 4-8 illustrates how Receive Data Blocks are stored within the dual-port RAM, while in the Sequential Mode of operation.

The Channel *x* Receive Error Count Register (see 4-42) is updated with every invalid Word, which is stored. The Start and End pointers set up the buffer size. The Receive Data Storage will stop when the end pointer is reached or will wrap around to the beginning of the buffer, depending upon the condition of the Receive Wrap Around bit in the Channel *x* Configuration Register (see 4-45). The Time Tag resolution is 10μsec/bit.

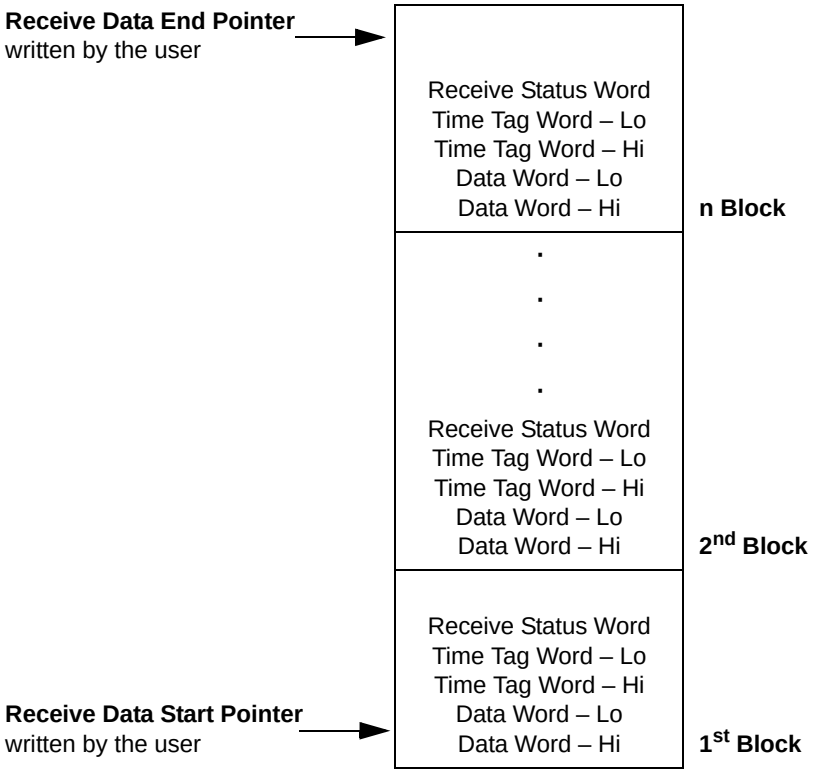


Figure 4-8 Receive Sequential Mode Buffer Structure

RECEIVE DATA WORD FORMAT

The received ARINC Word is stored as two 16-bit Words within the memory (Hi-word followed by a Lo-word).

The numbers shown within the two Words represent the ARINC bit numbers.

32-Bit ARINC Word Receive Format

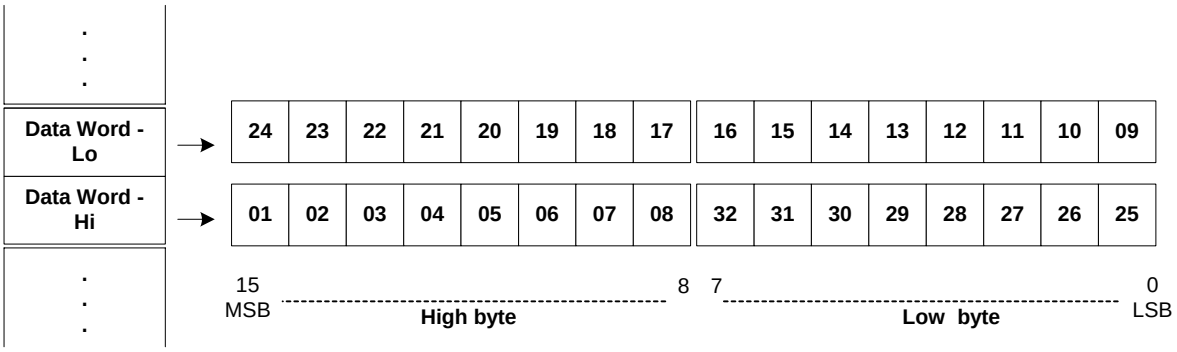


Figure 4-9 32-bit Receive Data Word Format

Note: 1. The ARINC Word bits are received in the following order:

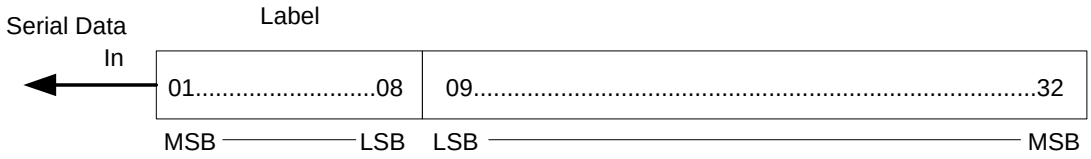


Figure 4-10 32-bit ARINC Word Order Bit

2. Bits 09 through 32 are ordered from LSB to MSB (as opposed to the Label field which is organized from MSB to LSB). For this reason, in the Data Block the Hi-word is first, followed by the Lo-word, with the Label and the ARINC field 32 through 25 in the Hi-word, and bits 24 through 09, in the Lo-word.

TIME TAG WORD FORMAT

The Time Tag is a 32-bit Word made up of two 16-bit Words: Time Tag-Hi and Time Tag-Lo.

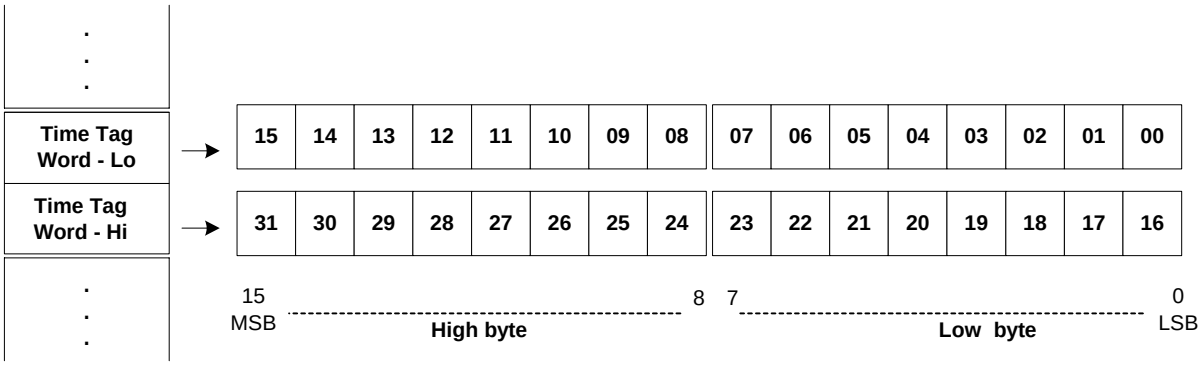


Figure 4-11 Time Tag Word Format

Note: There is latency between the time a Word is received on the bus and the time that Word is recorded in dual-port RAM. The number of channels and data rate of these channels affects this latency. The Time Tag reflects the time the Word is written to dual-port RAM rather than the time the Word is received over the bus. In no event will this latency exceed a single Hi-speed Word time of 360 microseconds.

RECEIVE SEQUENTIAL MODE STATUS WORD

Bit	Bit Name	Description
12-15	**Reserved**	
08-11	**Merge Channel ID Code** ***(Merge Mode only)***	0000 – Data received over Channel 0 0001 – Data received over Channel 1 0010 – Data received over Channel 2 0011 – Data received over Channel 3 0100 – Data received over Channel 4 0101 – Data received over Channel 5 0110 – Data received over Channel 6 0111 – Data received over Channel 7 1000 – Data received over Channel 8 1001 – Data received over Channel 9 **Note**: Channel ID Code: bit 8 = LSB Channel ID Code: bit 11 = MSB
07	**Valid Word**	1 = The Received ARINC word was valid in all respects (Global bit). 0 = Not a valid Word
06	**Reserved**	
05	**Gap (Sync) Time Error**	1 = Gap (Sync) Time Error occurred between Words (less than a 4 bit times between Words. 0 = No error
04	**Invalid Coding Error**	1 = Bit level coding error was detected in the ARINC Word 0 = No error
03	**Parity Error**	1 = A parity error was detected in the ARINC Word. 0 = No error
02	**Lo Bit Count / Invalid Word Error**	1 = A Lo Bit Count or a Null bit Error was detected in the ARINC Word. 0 = No error
01	**Hi Bit Count Error**	1 = A Hi Bit Count or a Null bit Error was detected in the ARINC Word. 0 = No error
00	**Word Received**	1 = Data is in memory. This bit is cleared while data is in the process of being updated. 0 = No received Word

Receive Sequential Mode Status Word

RECEIVE SEQUENTIAL MODE FILTER TABLE DIAGRAM

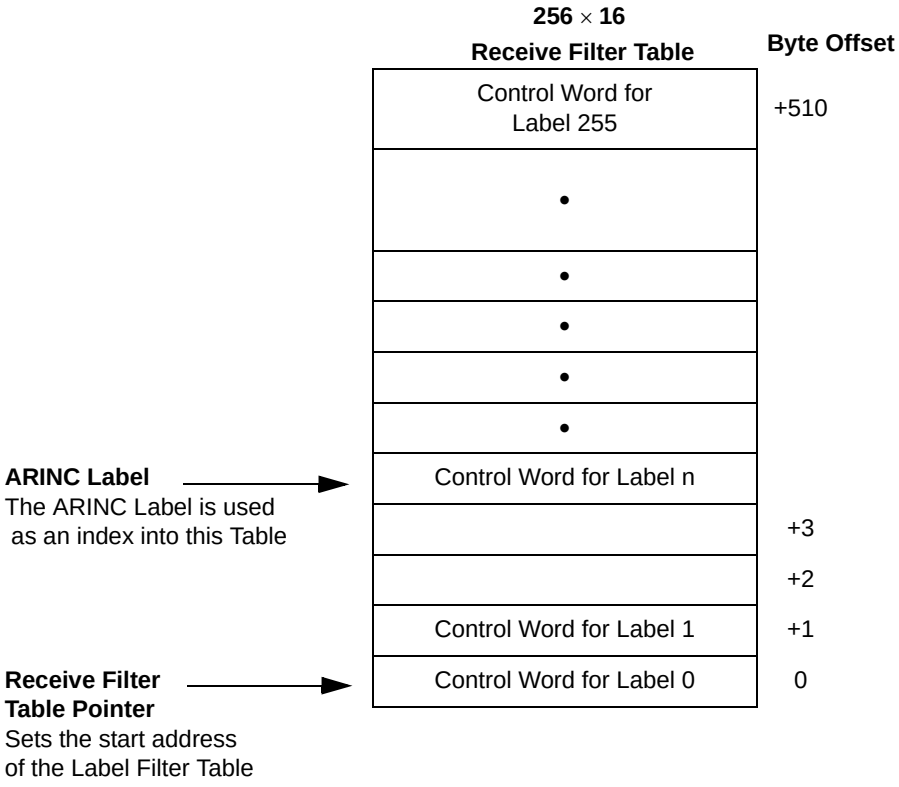


Figure 4-12 Receive Sequential Mode Filter Table Diagram

Bit	Description
02-15	Reserved
01	1 = Interrupt 0 = Don't Interrupt
00	1 = Store Word 0 = Don't Store

Label Control Word Structure (Write)

4.4.2 Look-up Table Mode Operation

In Look-up Table mode, the Word's Label is used by the card as an offset to a 256-word Look-up Table. The Table is programmed by the user with address pointers as to where to write the Receive Data Block. Each Block contains a:

- 32-bit ARINC Word,
- 32-bit Time Tag
- Error Count Word
- Status Word

The 256-word Table can be placed anywhere within the memory via a user-programmable Receive Look-up Table Start Address Register.

The user has the ability to monitor the operational status of each channel and to be interrupted on various events. In addition, there exist pollable registers that can be used with or instead of interrupt processing.

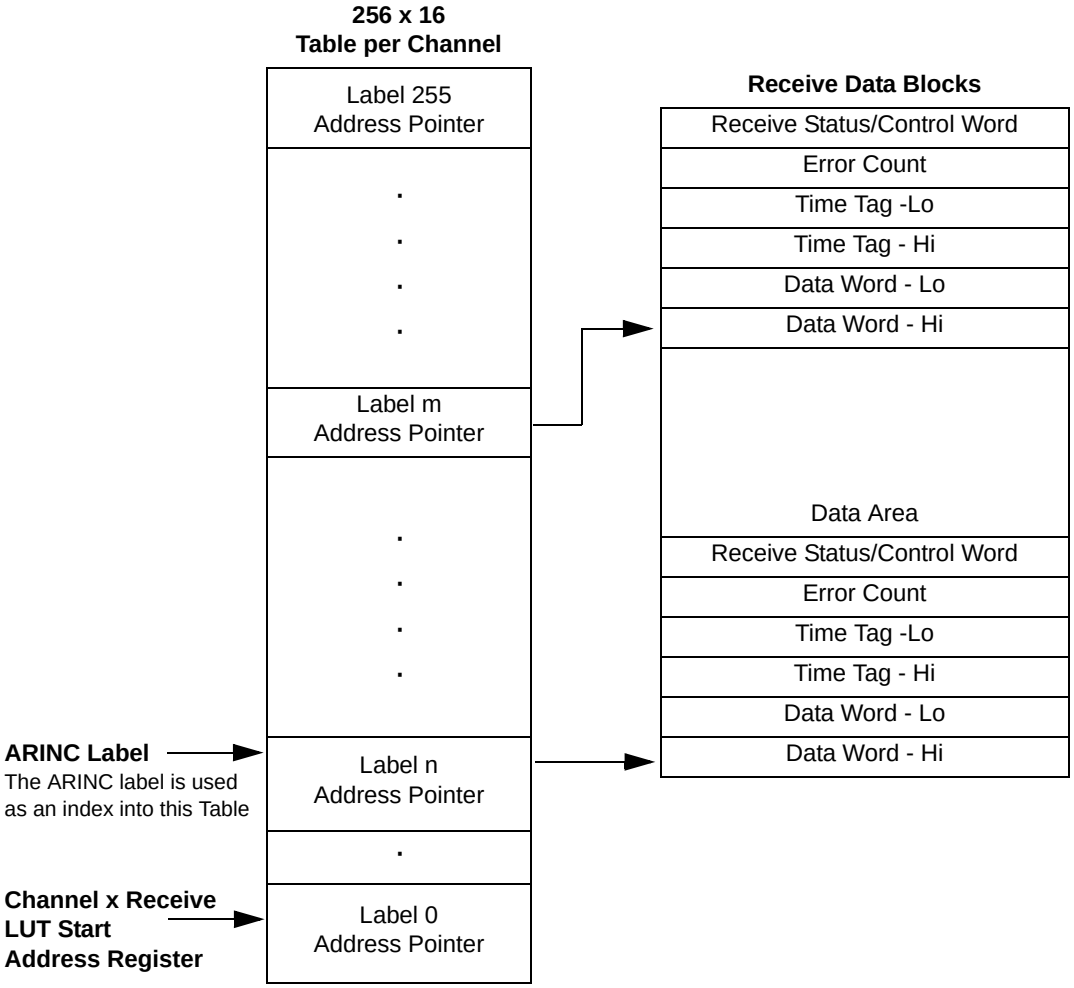


Figure 4-13 Receive Look-up Table Structure

RECEIVE DATA BLOCK DESCRIPTION

The Receive Data Block components are:

Data Word The ARINC Data Word is stored as two 16-bit Words with the same format - see **Receive Data Word Format** on page 4-24.

Time Tag Word The Time Tag Word is stored in two 16-bit Words with the same format - see **Time Tag Word Format** on page 4-25.

Error Count Word The Error Count Word indicates the number of error Words received on a particular Label.

Look-up Table – Receive Status / Control Word

	Bit	Bit Name	Description
Control Byte	**15**	Enable Label Interrupt	Enables the 'interrupt on Label received' capability. This bit is used in conjunctions with the Channel x Interrupt/Trigger Condition Register
	08–14	Reserved	Set to 0
Status Byte	**07**	Valid Word	1 = The Received ARINC Word was valid in all respects (Global bit) 0 = Not a valid Word
	06	Reserved	Set to 0
	05	Gap (Sync) Time Error	1 = Gap (Sync) Time Error occurred between Words (less than 4 bit times between Words.) 0 = No error
	04	Invalid Coding Error	1 = Bit level coding error was detected in the ARINC Word 0 = No error
	03	Parity Error	1 = A parity error was detected in the ARINC Word 0 = No error
	02	Lo Bit Count/ In Valid Word Error	1 = A Lo Bit Count or a Null bit error was detected in the ARINC Word 0 = No error
	01	Hi Bit Count Error	1 = A Hi Bit Count or a Null bit error was detected in the ARINC Word 0 = No error
	00	Word Received	

Look-up Table: Received Status/Control Byte

4.5 Channel Control Registers Maps

References to channels 5 – 9 are *only* for the *DAS-429PCMCIA/RT10*. For the Discrete channels on the *DAS-429PCMCIA/RT6D4*, which replace channels 5–9, see **Chapter 5: DAS-429PCMCIA/RT6D4 Operation & Control Registers**

4.5.1 Channel 0 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FD20-0FD22 H
Channel 0 Scratch Buffer End (W)	0FD24 H
Channel 0 Scratch Buffer Start (W)	0FD26 H
Channel 0 Status Register (R)	0FD28 H
Channel 0 Interrupt / Trigger Conditions (W)	0FD2A H
Reserved	0FD2C H
Channel 0 Transmit Loop Counter (W)	0FD2E H
Channel 0 Transmit Instruction Counter (W)	0FD30 H
Channel 0 Transmit Instruction Stack Pointer (W)	0FD32 H
Channel 0 Receive Label Trigger (W)	0FD34 H
Channel 0 Receive Error Count (R/W)	0FD36 H
Channel 0 Receive Interval Counter Trigger (W)	0FD38 H
Reserved	0FD3A H
Channel 0 Receive Data Word Counter Trigger (W)	0FD3C H
Channel 0 Receive Buffer Wraparound (W)	0FD3E H
Channel 0 Receive/Transmit Data Word Count (R)	0FD40 H
Channel 0 Receive Filter Table Start Address (W)	0FD42 H
Channel 0 Receive Look-up Table Start Address (W)	0FD44 H
Channel 0 Receive Data Current Pointer (R)	0FD46 H
Channel 0 Receive Data End Pointer (W)	0FD48 H
Channel 0 Receive Data Start Pointer (W)	0FD4A H
Reserved	0FD4C H
Channel 0 Configuration (W)	0FD4E H

Figure 4-14 Channel 0 Control Register Block Map

4.5.2 Channel 1 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FD50-0FD52 H
Channel 1 Scratch Buffer End (W)	0FD54 H
Channel 1 Scratch Buffer Start (W)	0FD56 H
Channel 1 Status Register (R)	0FD58 H
Channel 1 Interrupt / Trigger Conditions (W)	0FD5A H
Reserved	0FD5C H
Channel 1 Transmit Loop Counter (W)	0FD5E H
Channel 1 Transmit Instruction Counter (W)	0FD60 H
Channel 1 Transmit Instruction Stack Pointer (W)	0FD62 H
Channel 1 Receive Label Trigger (W)	0FD64 H
Channel 1 Receive Error Count (R/W)	0FD66 H
Channel 1 Receive Interval Counter Trigger (W)	0FD68 H
Reserved	0FD6A H
Channel 1 Receive Data Word Counter Trigger (W)	0FD6C H
Channel 1 Receive Buffer Wraparound (W)	0FD6E H
Channel 1 Receive/Transmit Data Word Count (R)	0FD70 H
Channel 1 Receive Filter Table Start Address (W)	0FD72 H
Channel 1 Receive Look-up Table Start Address (W)	0FD74 H
Channel 1 Receive Data Current Pointer (R)	0FD76 H
Channel 1 Receive Data End Pointer (W)	0FD78 H
Channel 1 Receive Data Start Pointer (W)	0FD7A H
Reserved	0FD7C H
Channel 1 Configuration (W)	0FD7E H

Figure 4-15 Channel 1 Control Register Block Map

4.5.3 Channel 2 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FD80-0FD82 H
Channel 2 Scratch Buffer End (W)	0FD84 H
Channel 2 Scratch Buffer Start (W)	0FD86 H
Channel 2 Status Register (R)	0FD88 H
Channel 2 Interrupt / Trigger Conditions (W)	0FD8A H
Reserved	0FD8C H
Channel 2 Transmit Loop Counter (W)	0FD8E H
Channel 2 Transmit Instruction Counter (W)	0FD90 H
Channel 2 Transmit Instruction Stack Pointer (W)	0FD92 H
Channel 2 Receive Label Trigger (W)	0FD94 H
Channel 2 Receive Error Count (R/W)	0FD96 H
Channel 2 Receive Interval Counter Trigger (W)	0FD98 H
Reserved	0FD9A H
Channel 2 Receive Data Word Counter Trigger (W)	0FD9C H
Channel 2 Receive Buffer Wraparound (W)	0FD9E H
Channel 2 Receive/Transmit Data Word Count (R)	0FDA0 H
Channel 2 Receive Filter Table Start Address (W)	0FDA2 H
Channel 2 Receive Look-up Table Start Address (W)	0FDA4 H
Channel 2 Receive Data Current Pointer (R)	0FDA6 H
Channel 2 Receive Data End Pointer (W)	0FDA8 H
Channel 2 Receive Data Start Pointer (W)	0FDAA H
Reserved	0FDAC H
Channel 2 Configuration (W)	0FDAE H

Figure 4-16 Channel 2 Control Register Block Map

4.5.4 Channel 3 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FDB0-0FDB2 H
Channel 3 Scratch Buffer End (W)	0FDB4 H
Channel 3 Scratch Buffer Start (W)	0FDB6 H
Channel 3 Status Register (R)	0FDB8 H
Channel 3 Interrupt / Trigger Conditions (W)	0FDBA H
Reserved	0FDBC H
Channel 3 Transmit Loop Counter (W)	0FDBE H
Channel 3 Transmit Instruction Counter (W)	0FDC0 H
Channel 3 Transmit Instruction Stack Pointer (W)	0FDC2 H
Channel 3 Receive Label Trigger (W)	0FDC4 H
Channel 3 Receive Error Count (R/W)	0FDC6 H
Channel 3 Receive Interval Counter Trigger (W)	0FDC8 H
Reserved	0FDCA H
Channel 3 Receive Data Word Counter Trigger (W)	0FDCC H
Channel 3 Receive Buffer Wraparound (W)	0FDCE H
Channel 3 Receive/Transmit Data Word Count (R)	0FDD0 H
Channel 3 Receive Filter Table Start Address (W)	0FDD2 H
Channel 3 Receive Look-up Table Start Address (W)	0FDD4 H
Channel 3 Receive Data Current Pointer (R)	0FDD6 H
Channel 3 Receive Data End Pointer (W)	0FDD8 H
Channel 3 Receive Data Start Pointer (W)	0FDDA H
Reserved	0FDDC H
Channel 3 Configuration (W)	0FDDE H

Figure 4-17 Channel 3 Control Register Block Map

4.5.5 Channel 4 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FDE0-0FDE2 H
Channel 4 Scratch Buffer End (W)	0FDE4 H
Channel 4 Scratch Buffer Start (W)	0FDE6 H
Channel 4 Status Register (R)	0FDE8 H
Channel 4 Interrupt / Trigger Conditions (W)	0FDEA H
Reserved	0FDEC H
Channel 4 Transmit Loop Counter (W)	0FDEE H
Channel 4 Transmit Instruction Counter (W)	0FDF0 H
Channel 4 Transmit Instruction Stack Pointer (W)	0FDF2 H
Channel 4 Receive Label Trigger (W)	0FDF4 H
Channel 4 Receive Error Count (R/W)	0FDF6 H
Channel 4 Receive Interval Counter Trigger (W)	0FDF8 H
Reserved	0FDFA H
Channel 4 Receive Data Word Counter Trigger (W)	0FDFC H
Channel 4 Receive Buffer Wraparound (W)	0FDFE H
Channel 4 Receive/Transmit Data Word Count (R)	0FE00 H
Channel 4 Receive Filter Table Start Address (W)	0FE02 H
Channel 4 Receive Look-up Table Start Address (W)	0FE04 H
Channel 4 Receive Data Current Pointer (R)	0FE06 H
Channel 4 Receive Data End Pointer (W)	0FE08 H
Channel 4 Receive Data Start Pointer (W)	0FE0A H
Reserved	0FE0C H
Channel 4 Configuration (W)	0FE0E H

Figure 4-18 Channel 4 Control Register Block Map

4.5.6 Channel 5 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FE10-0FE12 H
Channel 5 Scratch Buffer End (W)	0FE14 H
Channel 5 Scratch Buffer Start (W)	0FE16 H
Channel 5 Status Register (R)	0FE18 H
Channel 5 Interrupt / Trigger Conditions (W)	0FE1A H
Reserved	0FE1C H
Channel 5 Transmit Loop Counter (W)	0FE1E H
Channel 5 Transmit Instruction Counter (W)	0FE20 H
Channel 5 Transmit Instruction Stack Pointer (W)	0FE22 H
Channel 5 Receive Label Trigger (W)	0FE24 H
Channel 5 Receive Error Count (R/W)	0FE26 H
Channel 5 Receive Interval Counter Trigger (W)	0FE28 H
Reserved	0FE2A H
Channel 5 Receive Data Word Counter Trigger (W)	0FE2C H
Channel 5 Receive Buffer Wraparound (W)	0FE2E H
Channel 5 Receive/Transmit Data Word Count (R)	0FE30 H
Channel 5 Receive Filter Table Start Address (W)	0FE32 H
Channel 5 Receive Look-up Table Start Address (W)	0FE34 H
Channel 5 Receive Data Current Pointer (R)	0FE36 H
Channel 5 Receive Data End Pointer (W)	0FE38 H
Channel 5 Receive Data Start Pointer (W)	0FE3A H
Reserved	0FE3C H
Channel 5 Configuration (W)	0FE3E H

Figure 4-19 Channel 5 Control Register Block Map

4.5.7 Channel 6 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FE40 H 0FE42 H 0FE44 H 0FE46 H
Channel 6 Status Register (R)	0FE48 H
Channel 6 Interrupt / Trigger Conditions (W)	0FE4A H
Reserved	0FE4C H 0FE4E H 0FE50 H 0FE52 H
Channel 6 Receive Label Trigger (W)	0FE54 H
Channel 6 Receive Error Count (R/W)	0FE56 H
Channel 6 Receive Interval Counter Trigger (W)	0FE58 H
Reserved	0FE5A H
Channel 6 Receive Data Word Counter Trigger (W)	0FE5C H
Channel 6 Receive Buffer Wraparound (W)	0FE5E H
Channel 6 Receive/Transmit Data Word Count (R)	0FE60 H
Channel 6 Receive Filter Table Start Address (W)	0FE62 H
Channel 6 Receive Look-up Table Start Address (W)	0FE64 H
Channel 6 Receive Data Current Pointer (R)	0FE66 H
Channel 6 Receive Data End Pointer (W)	0FE68 H
Channel 6 Receive Data Start Pointer (W)	0FE6A H
Reserved	0FE6C H
Channel 6 Configuration (W)	0FE6E H

Figure 4-20 Channel 6 Control Register Block Map

4.5.8 Channel 7 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FE70 H 0FE72 H 0FE74 H 0FE76 H
Channel 7 Status Register (R)	0FE78 H
Channel 7 Interrupt / Trigger Conditions (W)	0FE7A H
Reserved	0FE7C H 0FE7E H 0FE80 H 0FE82 H
Channel 7 Receive Label Trigger (W)	0FE84 H
Channel 7 Receive Error Count (R/W)	0FE86 H
Channel 7 Receive Interval Counter Trigger (W)	0FE88 H
Reserved	0FE8A H
Channel 7 Receive Data Word Counter Trigger (W)	0FE8C H
Channel 7 Receive Buffer Wraparound (W)	0FE8E H
Channel 7 Receive/Transmit Data Word Count (R)	0FE90 H
Channel 7 Receive Filter Table Start Address (W)	0FE92 H
Channel 7 Receive Look-up Table Start Address (W)	0FE94 H
Channel 7 Receive Data Current Pointer (R)	0FE96 H
Channel 7 Receive Data End Pointer (W)	0FE98 H
Channel 7 Receive Data Start Pointer (W)	0FE9A H
Reserved	0FE9C H
Channel 7 Configuration (W)	0FE9E H

Figure 4-21 Channel 7 Control Register Block Map

4.5.9 Channel 8 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FEA0 H 0FEA2 H 0FEA4 H 0FEA6 H
Channel 8 Status Register (R)	0FEA8 H
Channel 8 Interrupt / Trigger Conditions (W)	0FEAA H
Reserved	0FEAC H 0FEAE H 0FEE0 H 0FEB2 H
Channel 8 Receive Label Trigger (W)	0FEB4 H
Channel 8 Receive Error Count (R/W)	0FEB6 H
Channel 8 Receive Interval Counter Trigger (W)	0FEB8 H
Reserved	0FEBA H
Channel 8 Receive Data Word Counter Trigger (W)	0FEBC H
Channel 8 Receive Buffer Wraparound (W)	0FEBE H
Channel 8 Receive/Transmit Data Word Count (R)	0FEC0 H
Channel 8 Receive Filter Table Start Address (W)	0FEC2 H
Channel 8 Receive Look-up Table Start Address (W)	0FEC4 H
Channel 8 Receive Data Current Pointer (R)	0FEC6 H
Channel 8 Receive Data End Pointer (W)	0FEC8 H
Channel 8 Receive Data Start Pointer (W)	0FECA H
Reserved	0FECC H
Channel 8 Configuration (W)	0FECE H

Figure 4-22 Channel 8 Control Register Block Map

4.5.10 Channel 9 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FED0 H 0FED2 H 0FED4 H 0FED6 H
Channel 9 Status Register (R)	0FED8 H
Channel 9 Interrupt / Trigger Conditions (W)	0FEDA H
Reserved	0FEDC H 0FEDE H 0FEE0 H 0FEE2 H
Channel 9 Receive Label Trigger (W)	0FEE4 H
Channel 9 Receive Error Count (R/W)	0FEE6 H
Channel 9 Receive Interval Counter Trigger (W)	0FEE8 H
Reserved	0FEEA H
Channel 9 Receive Data Word Counter Trigger (W)	0FEEC H
Channel 9 Receive Buffer Wraparound (W)	0FEEE H
Channel 9 Receive/Transmit Data Word Count (R)	0FEF0 H
Channel 9 Receive Filter Table Start Address (W)	0FEF2 H
Channel 9 Receive Look-up Table Start Address (W)	0FEF4 H
Channel 9 Receive Data Current Pointer (R)	0FEF6 H
Channel 9 Receive Data End Pointer (W)	0FEF8 H
Channel 9 Receive Data Start Pointer (W)	0FEFA H
Reserved	0FEFC H
Channel 9 Configuration (W)	0FEFE H

Figure 4-23 Channel 9 Control Register Block Map

4.6 Channel Control Register Definitions

References to channels 5 – 9 are *only* for the *DAS-429PCMCIA/RT10*. For the Discrete channels on the *DAS-429PCMCIA/RT6D4*, which replace channels 5–9, see **Chapter 5: DAS-429PCMCIA/RT6D4 Operation & Control Registers**.

4.6.1 Channel x Scratch Buffer End Register — Write

Data Rate Mode

For transmission in Data Rate Mode, the Channel *x* Scratch Buffer End Register contains the end address of the scratch buffer that must be assigned by the user. See **Channel x Scratch Buffer Start Register** on page 4-40.

4.6.2 Channel x Scratch Buffer Start Register — Write

Data Rate Mode

For transmission in Data Rate Mode, the user must allocate a scratch buffer for use by the firmware. Its length must be at least (Transmit Instruction Counter × 10 + 4) bytes. If the buffer is not long enough, the channel will turn itself off without transmitting.

The Channel *x* Scratch Buffer Start Register contains the start address of this buffer. The address must be a word boundary.

4.6.3 Channel x Status Register — Read

The Channel *x* Status Register indicates the operational status of the channel. This register can be used to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts, the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. The user must reset status bits, by writing a 0 to this register.

Bit	Bit Name – Interrupt Cause
07-15	Reserved
06	Receive - Stopped on Buffer Full
05	Receive - Error Word Received
04	Receive - Data Word Count Trigger
03	Receive - Interval Count Trigger
02	Receive - Label Received
01	Transmit - End of Frame
00	Transmit - End of Block

Channel *x* Status Register

Look-up Mode

In Look-Up Mode, the Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the label's Control byte.

Sequential Mode

In Sequential Mode, the Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the Filter Table.

4.6.4 Channel x Interrupt/Trigger Condition Register — Write

The Channel *x* Interrupt/Trigger Condition Register sets the Interrupt and Trigger condition or conditions of the channel. The Trigger Conditions set a pulse on the External Trigger Output.

Note: The Trigger Condition Bits are only relevant to the -002 card, which supports External Trigger Output. For more information about this card, contact Customer Service.

Trigger Condition Bits 08–15		Interrupt Condition Bits 00–07	
Bit	**Bit Name**	**Bit**	**Bit Name**
15	Reserved	**07**	Reserved
14	Receive – Stopped on buffer full	**06**	Receive – Stopped on buffer full
13	Receive – Error Word received	**05**	Receive – Error Word received
12	Receive – Data Word Count Trigger [1]	**04**	Receive – Data Word Count Trigger [1]
11	Receive – Interval Count Trigger [2]	**03**	Receive – Interval Count Trigger [2]
10	Receive – Label Received [3]	**02**	Receive – Label Received [3]
09	Transmit – End of Frame	**01**	Transmit – End of Frame
08	Transmit – End of Block	**00**	Transmit – End of Block

Receive Merge Interval/Trigger Condition Register

1. To activate the Receive – Data Word Count Trigger interrupt or trigger, the Channel x Receive Data Word Counter Trigger register must also be set.
2. To activate the Receive – Interval Count Trigger interrupt or trigger, the Channel x Receive Interval Counter Trigger register must also be set.
3. The Receive – Label Received interrupt or trigger only occurs upon reception of a label, which has been marked for interrupt in a Filter Table (in Sequential Mode) or in a Control Byte (in Look-up Table Mode.

4.6.5 Channel x Transmit Loop Counter — Write

The Channel *x* Transmit Loop counter sets the number of times to execute the transmit instruction blocks (the frame): *N* Times or Continuous Loop. If the continuous value is selected, setting the related channel bit in the Global Start/ Stop Register to a 0 can terminate the channel's operation.

Bit	Value	
00–15	0000	= Continuous
	0001	= One time
	0002	= Two times
		•
		•
		•
	FFFF	65535 times

Channel *x* Transmit Loop Counter

4.6.6 Channel x Transmit Instruction Counter — Write

The Channel *x* Transmit Instruction Counter sets the number of Transmit Instruction blocks to process. These instruction blocks taken together comprise a frame.

4.6.7 Channel x Transmit Instruction Stack Pointer — Write

The Channel *x* Transmit Instruction Stack Pointer sets the starting address of the Transmit Instruction Stack**.** The address must be a word boundary within the Transmit Instruction Stack area. For example, to place the Transmit Instruction stack starting at location 0300 (H), write 0300 (H) to this register.

4.6.8 Channel x Receive Label Trigger Register — Write

Sequential Mode

The Channel *x* Receive Label Trigger Register is used in conjunction with the Receive Label Trigger bit in the Channel *x* Configuration Register (see **Channel x Configuration Register** on page 4-45). This register enables the reception and storage of data upon receipt of a unique ARINC label. The card will not store any ARINC words received prior to the first instance of this label.

Bit	Description
08–15	Set to 0
00–07	Trigger Label

Channel *x* Receive Label Trigger Register

4.6.9 Channel x Receive Error Count Register — Read/Write

Sequential Mode

The 16-bit Channel *x* Receive Error Count Register indicates the number of errors received on a particular channel. To reset the register, write 0000 to it.

4.6.10 Channel x Receive Interval Counter Trigger Register — Write

Sequential Mode

The Channel *x* Receive Interval Counter Trigger Register allows the user to generate an interrupt and set a flag upon reception of every *N* number of words, where *N* is the value written to this register. For example, to request an interrupt after every five ARINC words, write 0005 (H) to this register.

To generate an interrupt or a trigger, the appropriate bit must also be set in the Channel *x* Interrupt / Trigger Condition Register (see **Channel x Interrupt/Trigger Condition Register** on page 4-41).

4.6.11 Channel x Receive Data Word Counter Trigger Registers — Write

The Channel *x* Receive Data Word Counter Trigger Register lets the user generate an interrupt and set a flag, which indicates when a specific number of words have been received (1-65535). To generate an interrupt, the appropriate bit must also be set in the Channel *x* Interrupt/Trigger Condition Register (see **Channel x Interrupt/Trigger Condition Register** on page 4-41).

Note: This trigger is set when the value in the Receive Data Word Counter matches the value set in this register.

4.6.12 Channel x Receive Buffer Wraparound Register — Write

The Channel *x* Receive Buffer Wraparound Register contains 2 bits for synchronization with the host.

Bit	Description
15	1 = Multiple Wraparound - Data Lost
14	1 = Single Wraparound since last data read
00-13	0

Channel *x* Receive Buffer Wraparound Register

Note: Excalibur software drivers handle these bits. If these drivers, are used, they do not need to be modified.

The user should clear bit 14 each time the first word of the buffer is read. When the buffer wraps around bit 14 is checked. If bit 14 is '0', the card sets the bit to indicate a Single Wrap Around ('1'). If bit 14 is '1', the card sets bit 15 to indicate a Multiple Wraparound mode ('1') has occurred.

4.6.13 Channel x Receive Data Word Count Register — Read

Sequential Mode

The Channel *x* Receive Data Word Count Register indicates the number of ARINC words received (0-65535). This register wraps around to 0 after it reaches 65535. The user may reset the register to 0, only when the channel is stopped.

4.6.14 Channel x Receive Filter Table Start Address — Write

Sequential Mode

The Channel *x* Receive Filter Table Start Address sets the Start Address of the 256 × 8 Label Filter Table as described in section **4.4.1 Sequential and Merge Modes** on page 4-22. The address must be a word boundary. It is valid for several channels to use the same Filter Table.

This table is valid only if the Channel *x* Configuration Register Enable Receive Filter Table bit is set. (See bit 09 in the **Channel x Configuration Register** on page 4-45.)

4.6.15 Channel x Receive Look-up Table Start Address — Write

Look-up Table Mode

The Channel *x* Receive Look-Up Table Start Address sets the start address of the 256 × 16 Receive Look-Up Table (see bit 05 in the **Channel x Configuration Register** on page 4-45). The address must be a word boundary.

This address points to the *first* location of the Look-Up Table. The card stores one ARINC data block for each Label received. The data block contains: 32-bit ARINC word, 32-bit Time Tag, and the 16-bit Receive Status Word. The subsequent reception and storage of another ARINC word will overwrite the Data Block with the same ARINC Label.

4.6.16 Channel x Receive Data Current Pointer — Read

Sequential Mode

In Sequential Mode the Channel *x* Receive Data Current Pointer indicates the address where the next ARINC receive word is to be placed in the buffer. This pointer value is incremented after the entire receive block (ARINC word, Time Tag, and Status) is written into memory.

Look-up Table Mode

In Look-Up Table Mode this register contains the address of the last ARINC receive word written to the receive area.

4.6.17 Channel x Receive Data End Pointer — Write

Sequential Mode

The Channel *x* Receive Data End Pointer sets the end address of the Receive Data buffer. The address must be a word boundary. The data will wrap around or stop when the buffer is full, (when the End Address is reached), depending upon the contents of the Receive Wrap Around control bit in the Channel *x* Configuration Register.

4.6.18 Channel x Receive Data Start Pointer — Write

Sequential Mode

The Channel *x* Receive Data Start Pointer Register sets the start address of the Receive Data buffer. The address must be a word boundary within the Receive Data Blocks area.

Example: To cause the Channel *x* Receive Data Buffer to begin at address 001A0 (H), write 01A0 (H) to this register.

4.6.19 Channel x Configuration Register — Write

The Channel *x* Configuration Register sets up various run parameters for each channel. Bits that are not used (for example, receive-related bits while operating as a transmitter) are ignored by the card.

Bit	Bit Name	Description
11-15	**Reserved**	Set to 0
10	**Extended Time Mode**	1 = Extended Time Mode selected 0 = Standard Time Mode selected When Extended Time Mode is selected, the Interblock Time/Data Rate is doubled on the bus. See **Interblock Time/Data Rate Word** on page 4-20. This bit is only relevant if Extended Time Mode is supported by the firmware. See **Card Status Register** on page 4-11.
09	**Enable Receive Filter Table**	1 = Enable Filter Table (Stores labels per table) 0 = Disables table. Stores all labels.
08	**Transmit Mode Select**	1 = Data Rate mode (per data block) 0 = Interblock Gap Time mode See section **4.3 Transmit Channel Operation** on page 4-17
07	**Receive Label Trigger**	1 = Start data storage upon receipt of Label xx. See **Channel x Receive Label Trigger Register** on page 4-42. 0 = Receive stores data without Start Label Trigger
06	**Receive Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receive wraps around the data within the block. (This bit is used in Sequential Storage Mode only.)
05	**Receive Storage Mode**	1 = Sequential Storage Mode 0 = Look-up Table Mode (see **Channel x Receive Look-up Table Start Address** on page 4-44).
04	**Parity: Even/Odd**	1 = Even 0 = Odd - Standard ARINC Mode
03	**Parity: On/Off**	1 = Off 0 = On
02	**Transmit Rise/ Fall Time**	1 = Lo Speed (10 +/- 5μsec.) 0 = Hi Speed (1.5 +/- 0.5μsec.)
00-01	**Bit Rate**	If the Programmable Bit Rate is selected then the bit rate is defined by the global **Programmable Bit Rate Register** (see page 4-10).

Bit 01	Bit 00	Channel Bit rate
0	0	12.5 KHz – Lo Speed
0	1	100 KHz – Hi Speed
1	0	Programmable
1	1	Undefined

Channel *x* Configuration Register

The Channel *x* Configuration Register can only be written to when *all* the channels are turned off (via the Start/Stop Register).

The card should be started (via the Start/Stop Register) only after a minimum of 1msec from the time that the contents of the register have been modified.

All active Channel *x* Configuration Registers should be set up immediately following the card ID validation, before programming other parameters.

5 *DAS-429PCMCIA/RT6D4* Operation & Control Registers

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5.1 *DAS-429PCMCIA/RT6D4* Overview

The *DAS-429PCMCIA/RT6D4* card includes:

- Six programmable receive and transmit channels as in the *DAS-429PCMCIA/RT10*, see **Chapter 4: Card Operation** for descriptions of the control registers for these channels, and
- Four bidirectional discretes channels.

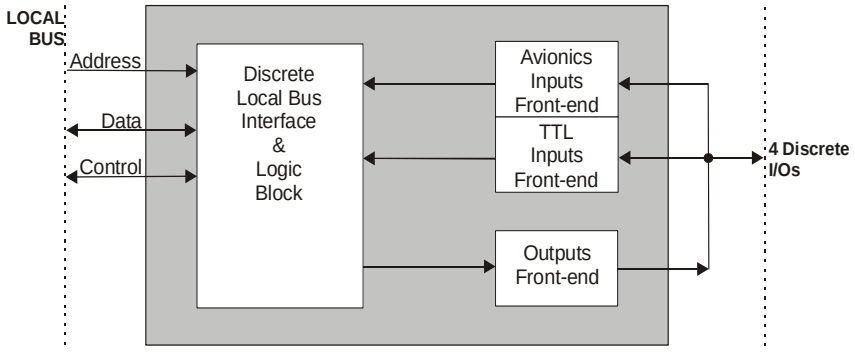

Figure 5-1 DAS-429PCMCIA/RT6D4 Block Diagram

5.2 Discrete Channel Voltage Levels and I/O Connections

5.2.1 Input Voltage Thresholds

The voltage thresholds for the *DAS-429PCMCIA/RT6D4* Discrete input channels are:

Type	Threshold Voltage (V)	Input Channel State
TTL	0 – 0.8	Low
	2.0 – 5.0	High
AVIONICS	0 – 3.0	Low
	7.5 – 32.0	High

Table 5-1 Input Voltage Thresholds

Note Only one type (TTL or Avionics voltage) can be applied to the input channels at one time. The voltage limits must not be exceeded.

5.2.2 Discrete I/O Connections

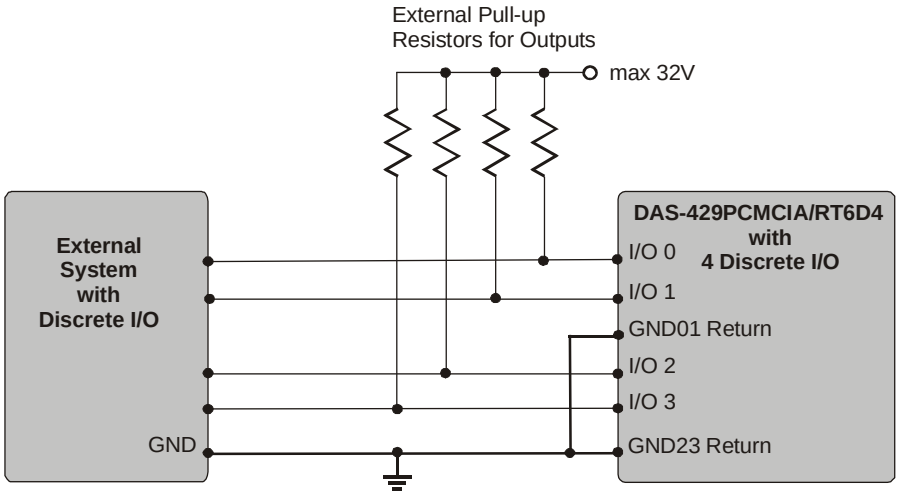

Figure 5-2 Discrete I/O Channels

5.3 Discrete Control Registers Map

The Discrete Control Registers are read/write and are reset to 0 unless otherwise stated.

Figure **5-3** illustrates the Control Registers.

Input Channel Register (Read only)	0FFA0 H
Threshold Register	0FFA2 H
Output Channel Register 0	0FFA4 H
Output Channel Register 1	0FFA6 H
Output Channel Register 2	0FFA8 H
Output Channel Register 3	0FFAA H
Reserved	0FFAC H
Start Register	0FFAE H
Reset Register (Write Only)	0FFB0 H
Trigger Mask Register	0FFB2 H
Trigger Value Register	0FFB4 H
Interrupt Pending Register (Read only)	0FFB6 H
Reset Interrupt Pending Register (Write only)	0FFB8 H
Trigger Destination Register	0FFBA H
Card Type Register	0FFBC H
Reserved Memory	00FBE – 0FFBE H

Figure 5-3 Discrete Control Registers Map

5.4 Discrete Control Registers Definitions

5.4.1 Input register — Address: 0FFA0 (H)

Read The Input Register stores the values received from each of the input channels (0–3). Either Avionics or TTL logic-levels are stored in this register, depending on the value of the Threshold Register, (see section **5.4.2 Threshold Register** on page 5-4)

As all the inputs are placed in a single register, all the channels can be polled in one read cycle.

Bit	Signal	Description
04-15	Reserved	
03	IN3	Logic-level voltage on input channel 3
02	IN2	Logic-level voltage on input channel 2
01	IN1	Logic-level voltage on input channel 1
00	IN0	Logic-level voltage on input channel 0

Input Register

Note:

1. When the card is *stopped,* all values in the Input register remain constant and are not effected by changes in the logic-level voltages on the Input channels
2. When the card is *started,* all the values in the Input register will be updated/ changed according to the logic-level voltages placed on the input channels. (See section **5.4.4 Start Register** on page 5-5.)

5.4.2 Threshold Register — Address: 0FFA2 (H)

The Threshold Register defines which type of logic-level voltage is present on the input channels.

Bit	Description
01-15	Reserved
00	Logic-level voltage present on the Input channels 0 = Avionics (0–32V) 1 = TTL (0–5V) **default value**

Threshold Register

5.4.3 Output Registers

Address: 0FFA4-0FFAA (H)

The Output Registers contain the values that will indicate the logic-level voltage to be supplied to the open collector, output channels.

Bit	Description	
01-15	Reserved	
00	Output signal 0 = Low 1 = High (floating) – **default value**	
	Address	Output
	0FFA4 (H)	Output 0
	0FFA6 (H)	Output 1
	0FFA8 (H)	Output 2
	0FFAA (H)	Output 3

Output Registers

Note: When the card is *stopped* all values in the Output registers can be altered but their value will not be placed on the output channels until the card is started.

When the card is *started,* all the voltage levels in the output channels will reflect the values in the Output registers. (See **5.4.4 Start Register** on page 5-5).

5.4.4 Start Register

Address: 0FFAE (H)

The Start Register controls the start/stop operation of the card.

Bit	Description
01-15	Reserved
00	Start/Stop operation 0 = Stop card: All values in the Input Register remain constant and are not effected by changes in the voltage levels on the input channels. The values in the Output Registers can be altered but their value will not be placed on the Output channels until the card is started. The value on the output channels will be dependent on the last value stored in the Output register before the card was stopped. No effect on all other registers. 1 = Start card: All values in the Input and Output registers can be updated and/or changed. No effect on other registers.

Start Register

5.4.5 Reset Register Address: 0FFB0 (H)

Write Writing any value to the Reset Register will cause a software reset to the card. A reset will cause all registers to restore the default values.

5.4.6 Trigger Mask Register Address: 0FFB2 (H)

The Trigger Mask Register defines which input channels are to be monitored for activity. When any of the masked inputs change, a trigger will be produced depending on the value of the **Trigger Value Register** on page 5-6. The output of the trigger is dependent on the **Trigger Destination Register** on page 5-7. The channel that produced the trigger is stored in the **Interrupt Pending Register** on page 5-7.

Bit	Description
04-15	Reserved
03	0 = Do not monitor channel 3 1 = Monitor channel 3
02	0 = Do not monitor channel 2 1 = Monitor channel 2
01	0 = Do not monitor channel 1 1 = Monitor channel 1
00	0 = Do not monitor channel 0 1 = Monitor channel 0

Trigger Mask Register

5.4.7 Trigger Value Register Address: 0FFB4 (H)

The Trigger Value Register defines if a trigger will be generated by a rising edge or a falling edge on the specific input channel.

Bit	Description
04-15	Reserved
03	0 = Rising edge on input channel 3 1 = Falling edge on input channel 3
02	0 = Rising edge on input channel 2 1 = Falling edge on input channel 2
01	0 = Rising edge on input channel 1 1 = Falling edge on input channel 1
00	0 = Rising edge on input channel 0 1 = Falling edge on input channel 0

Trigger Value Register

5.4.8 Interrupt Pending Register

Address: 0FFB6 (H)

Read Use the Interrupt Pending Register to identify which channel or channels produced a trigger and thus requested an interrupt/external trigger.

Bit	Description
04-15	Reserved
03	0 = No trigger generated by channel 3 1 = Trigger generated by channel 3
02	0 = No trigger generated by channel 2 1 = Trigger generated by channel 2
01	0 = No trigger generated by channel 1 1 = Trigger generated by channel 1
00	0 = No trigger generated by channel 0 1 = Trigger generated by channel 0

Interrupt Pending Register

5.4.9 Reset Interrupt Pending Register

Address: 0FFB8 (H)

Write Writing to the Reset Interrupt Pending Register will reset the corresponding bits of the Interrupt Pending Register.

Bit	Description
04-15	Reserved
00-03	Reset Pending 0 = No effect 1 = Reset the corresponding bit in the Interrupt Pending Register

Reset Interrupt Pending Register

Note: The Interrupt Pending Register bits are not cleared automatically, they must be reset with this register.

5.4.10 Trigger Destination Register

Address: 0FFBA (H)

Use the Trigger Destination Register to control where the trigger on the input, or inputs, is output.

Bit	Description		
02-15	Reserved		
00-01	Trigger Output		
	Bit 01	**Bit 00**	
	0	0	Not Connected
	0	1	Routed to interrupt line

Trigger Destination Register

5.4.11 Card Type Register

Address: 0FFBC H

Read The Card Type registers shows the card configuration.

Bit	Bit Name	
04–15	**Reserved**	
00–03	**Card type**	A = DAS-429PCMCIA/RT10
		D = DAS-429PCMCIA/RT6D4

Card Type Register

6 Mechanical and Electrical Specifications

Chapter 6 describes the mechanical and electrical specifications of the *DAS-429PCMCIA/RT[D]* card.

6.1 Connectors 6-1
6.1.1 DAS-429PCMCIA/RT10 and DAS-429PCMCIA/RT6D4 Adapter Cable 6-2
6.1.2 68-Pin PCMCIA Bus Connector Pinout 6-4
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6.1 Connectors

The *DAS-429PCMCIA/RT[D]* contains two connectors:

- 22-Pin ARINC 429 I/O Connector
- 68-Pin PCMCIA Bus Connector

Note: Each card is shipped with an adapter cable assembly.

The *DAS-429PCMCIA/RT[D]*-R option has cables soldered directly on to the PCMCIA PCB, exiting the card in the same location as the original 22-pin connector. The cables are “strain relieved” so that no force can be applied to the cable/PCB solder connections. In addition, the cable connections are hermetically sealed with epoxy potting compound, making the card and cable one inseparable entity.

6.1.1 DAS-429PCMCIA/RT10 and DAS-429PCMCIA/RT6D4 Adapter Cable

Excalibur provides adapter cables that convert the AMP I/O PCMCIA 22-pin connector to a standard D-type, female 25-pin connector with jack screws.

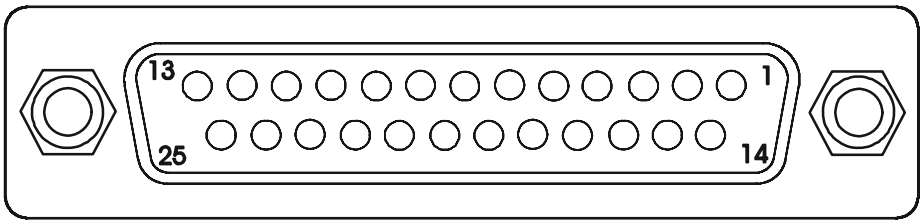


Figure 6-1 *DAS-429PCMCIA/RT[D]* Adapter Cable Connector - Front View

The *DAS-429PCMCIA/RT10* and *DAS-429PCMCIA/RT6D4* have different adapter cable connector pinouts. For the *DAS-429PCMCIA/RT10* see **Table 6-1** and for the *DAS-429PCMCIA/RT6D4* see **Table 6-2**.

DAS-429PCMCIA/RT10 Adaptor Cable Connector Pin Assignments And Description

Pin #	Signal Name	Description
1	CH0L	Channel 0 ARINC low line connection
2	CH1L	Channel 1 ARINC low line connection
3	CH2L	Channel 2 ARINC low line connection
4	CH3L	Channel 3 ARINC low line connection
5	CH4L	Channel 4 ARINC low line connection
6	GND	Ground, provided for cable shield connection
7	CH5L	Channel 5 ARINC low line connection
8	CH6L	Channel 6 ARINC low line connection
9	CH7L	Channel 7 ARINC low line connection
10	CH8L	Channel 8 ARINC low line connection
11	CH9L	Channel 9 ARINC low line connection
12-13		NC[a]
14	CH0H	Channel 0 ARINC high line connection
15	CH1H	Channel 1 ARINC high line connection
16	CH2H	Channel 2 ARINC high line connection
17	CH3H	Channel 3 ARINC high line connection
18	CH4H	Channel 4 ARINC high line connection
19	CH5H	Channel 5 ARINC high line connection
20	CH6H	Channel 6 ARINC high line connection
21	CH7H	Channel 7 ARINC high line connection
22	CH8H	Channel 8 ARINC high line connection
23	CH9H	Channel 9 ARINC high line connection
24-25		NC

Table 6-1 DAS-429PCMCIA/RT10 Adapter Cable Connector Pin Assignments and Description

a. NC = not connected

DAS-429PCMCIA/RT6D4 Adaptor Cable Connector Pin Assignments And Description

Pin #	Signal Name	Description
1	CH0L	Channel 0 ARINC low line connection
2	CH1L	Channel 1 ARINC low line connection
3	CH2L	Channel 2 ARINC low line connection
4	CH3L	Channel 3 ARINC low line connection
5	CH4L	Channel 4 ARINC low line connection
6	GND	Ground, provided for cable shield connection
7	CH5L	Channel 5 ARINC low line connection
8	GND01	Ground return for Discrete channels 0 and 1
9	VCC	5 Volt (can be used for TTL-level pull-ups)
10	GND23	Ground return for Discrete channels 2 and 3
11		NC[a]
12-13		NC
14	CH0H	Channel 0 ARINC high line connection
15	CH1H	Channel 1 ARINC high line connection
16	CH2H	Channel 2 ARINC high line connection
17	CH3H	Channel 3 ARINC high line connection
18	CH4H	Channel 4 ARINC high line connection
19	CH5H	Channel 5 ARINC high line connection
20	IOD0	Discrete I/O channel 0
21	IOD1	Discrete I/O channel 1
22	IOD2	Discrete I/O channel 2
23	IOD3	Discrete I/O channel 3
24-25		NC

Table 6-2 DAS-429PCMCIA/RT6D4 Adapter Cable Connector Pin Assignments and Description

a. NC = Not Connected

6.1.2 68-Pin PCMCIA Bus Connector Pinout

Pin #	Signal
1	GND
2	D3
3	D4
4	D5
5	D6
6	D7
7	CE1#
8	A10
9	OE#
10	A11
11	A9
12	A8
13	A13
14	A14
15	WE#
16	IREQ#
17	VCC
18	NC
19	A16
20	A15
21	A12
22	A7
23	A6
24	A5
25	A4
26	A3
27	A2
28	A1
29	A0
30	D0
31	D1
32	D2
33	GND
34	GND

Pin #	Signal
35	GND
36	CD1#
37	D11
38	D12
39	D13
40	D14
41	D15
42	CE2#
43	NC
44	NC
45	NC
46	A17
47	A18
48	NC
49	NC
50	NC
51	VCC
52	NC
53	NC
54	NC
55	NC
56	NC
57	NC
58	RESET
59	WAIT#
60	NC
61	REG#
62	NC
63	NC
64	D8
65	D9
66	D10
67	CD2#
68	GND

NC = Not Connected

6.2 Card Layout and Dimensions

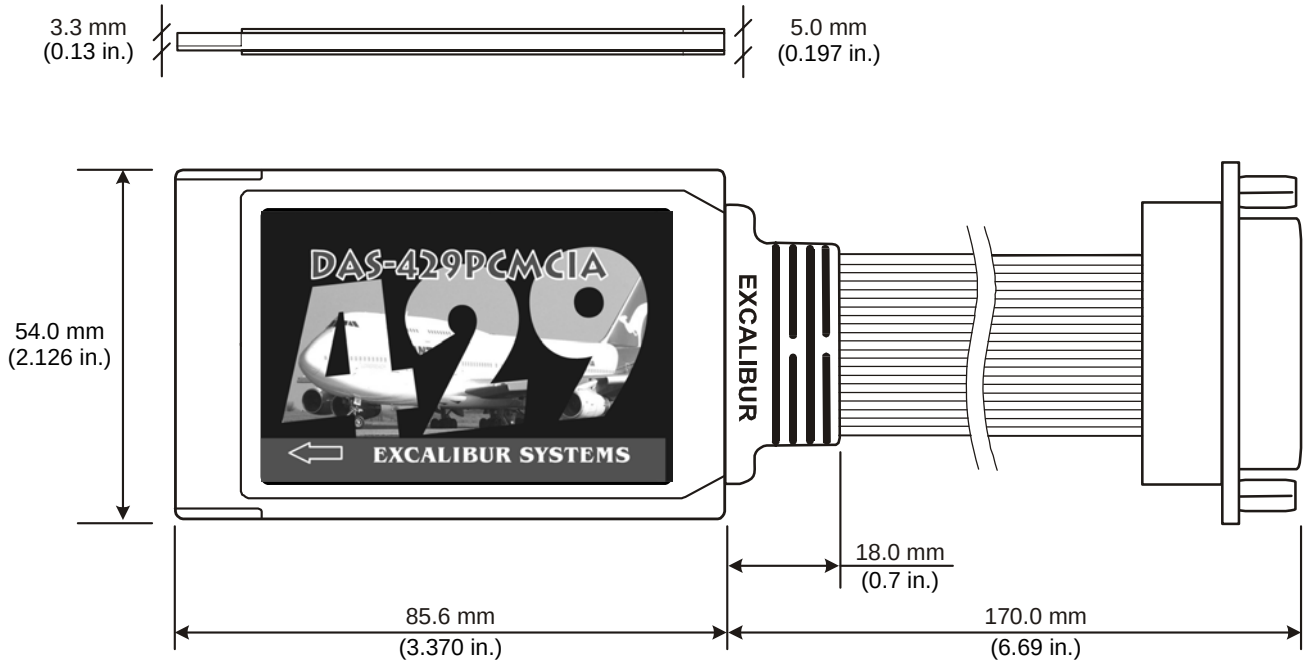


Figure 6-2 *DAS-429PCMCIA/RT[D]-R* Card Layout and Dimensions

6.3 Power Supply Requirements

The maximum power requirements for the *DAS-429PCMCIA/RT[D]* card are:

Standby (all channels receive)	+5V@200mA
With 1 transmit channel[a]	+5V@310mA
For each additional transmit channel,[a] add:	+5V@110mA

a. Transmitting at high speed with maximum load

7 Ordering Information

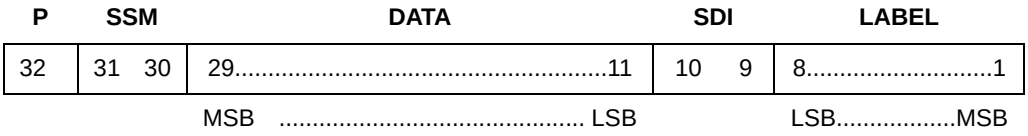
Chapter 7 provides the part numbers to use when ordering.

Basic Part #	Option	Description
DAS-429PCMCIA/RT10		ARINC 429 interface card with 6 channels that are independently configurable as receive or transmit, and 4 receive-only channels; with hardwired cable connection
DAS-429PCMCIA/RT6D4		ARINC 429 and Discrete interface card with 6 ARINC 429 channels that are independently configurable as receive or transmit, and 4 Discretes that are independently configurable as Input or Output; with hardwired cable connection
	-E	Add this suffix for the extended temperature option (-40° to +85° C)

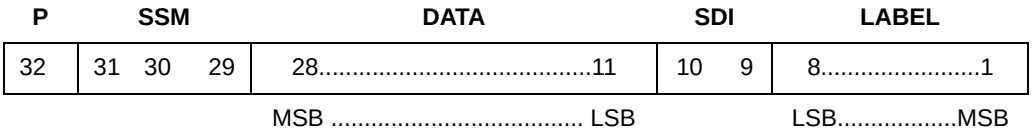
Appendix A ARINC 429 Basic Word Formats

All data sent over the ARINC bus is composed of 32-bit words. A number of different formats can be used, as the following diagrams show:

Format 1



Format 2



Format 3

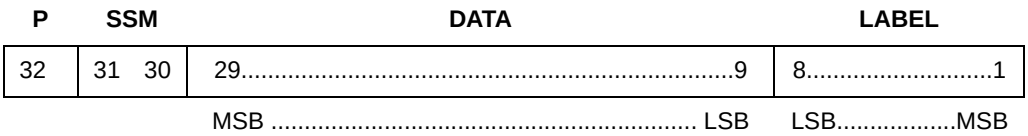


Figure 8-1 ARINC 429 Basic Word Formats

Key:

Field	Description
LABEL	Information identifier
SDI	Source/Destination Identifier bits
DATA	Information data: may be presented in one of the following formats
	BNR (Binary)
	BCD (Binary Coded Decimal)
	Discrete
	Maintenance and Acknowledgment
	Alpha Numeric (ISO Alphabet no.5)
SSM	Sign/Status Matrix bits
P	Parity bit (Odd parity)
LSB	Least Significant bit
MSB	Most Significant bit

Bits are transmitted starting with bit 1, the final bit transmitted is the parity bit, bit 32. The label is transmitted with the most significant bit first while the data is transmitted least significant bit first.

The **LABEL** is a octal value from 1 to 377 representing a particular type of data. Most labels are defined in the specification though some are reserved for future needs. Many labels are multiply defined in the specification based on the type of equipment being used.

The **SDI** field is used when a transmitter is connected to multiple receivers but not all data is meant to be used by all the receivers. In this case each receiver will be assigned an SDI value and will look only at labels that match its SDI value. While the specification calls for SDI 00 to be universally accepted a good deal of equipment appears to disregard this requirement.

The **DATA** field contains the actual data to be sent. A number of data formats are defined in the specification. Binary Coded Decimal (BCD) format uses each four bits to contain a single decimal digit. BNR data is a binary coding. For both data types the specification calls out the units, the resolution, the range, the number of bits used and how frequently the label should be sent. A discrete type has multiple single bit fields defined within a single label. A number of other formats are described in the specification.

SSM, which is sometime 3 bits long, is used for information which helps interpret the numeric value in the data field. Examples of SSM values might be Plus, North, East, Right, To or Above.

P is the parity bit. ARINC 429 calls for odd parity. The parity bit is the last bit sent over the bus.

Appendix B ARINC 429 Connection Precautions

Bppendix B describes connection precautions for ARINC 429 cards:

1. Verify the ARINC-429 line is not overloaded beyond the spec:

   Rload > 400 ohm

   Cload < 30,000 pF
2. Use shielded twisted pair wires with typical impedance of 60 to 80 Ohms.
3. Ensure that there is common ground between the connected systems in order to avoid potential differences.
4. Connect/Disconnect cables while the card is powered OFF or *not* transmitting at least.
5. Special care needs to be taken while applying probes of measuring instruments to avoid shorting out signals.

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August 2009, Rev A-2